Quartus Prime Pro Edition Software and Device Support Release Notes Version 15.1

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This document provides late-breaking information about the Altera® Quartus® Prime Pro Edition software release version 15.1.

Attention: The Quartus Prime Pro Edition software version 15.1 is a beta release. It is available for you to evaluate new features.

The Quartus II software is now the Quartus Prime software. The Quartus Prime software is available in three editions based on your design requirements: Pro, Standard, and Lite Edition.

- Quartus Prime Pro Edition—The Quartus Prime Pro Edition software is optimized to support the advanced features in Altera's next-generation FPGAs and SoCs, starting with the Arria® 10 device family.

  Use the Quartus Prime Pro Edition software if you are starting a new Arria 10 design or if your Arria 10 design requires features that are only available in the Quartus Prime Pro Edition software.

  The Quartus Prime Pro Edition software is free with an active Quartus Prime Standard Edition software license during beta release. Please contact your Altera sales representative for more details.
- Quartus Prime Standard Edition—The Quartus Prime Standard Edition software includes the most extensive support for Altera's latest device families and requires a subscription license.

  Use the Quartus Prime Standard Edition software for the following types of designs:

  - Designs that target non-Arria 10 devices.
  - Existing Arria 10 designs that you have created using the Subscription Edition of the Quartus II software.
  - Active Arria 10 designs that will go to production in the next 6 months

  For more information, refer to the *Quartus Prime Standard Edition Software and Device Support Release Notes Version 15.1*.
- Quartus Prime Lite Edition–The Quartus Prime Lite Edition provides an ideal entry point to Altera's high-volume device families and is available as a free download with no license required.

For information about operating system support, refer to the **readme.txt** file in your **altera/<*version number*>/quartus directory**.

Related Information

Quartus Prime Standard Edition Software and Device Support Release Notes Version 15.1

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New Features and Enhancements

The Quartus Prime Pro Edition software release version 15.1 includes the following new features and enhancements:

- Programming support for Arria 10 10AX115 ES3 devices.
- A Spectra-Q™ Hybrid Placer with advanced placement and routing algorithms for more predictable timing closure.
- A Spectra-Q Physical Synthesis feature for improved Fmax on designs that require high synthesis effort.
- A multi-corner timing visualization feature in the TimeQuest Timing Analyzer.
- A logic depth report for early design analysis.
- A Periphery to Core Placement and Routing Optimization feature.
- Expanded Spectra-Q Synthesis language support for IEEE standards, including SystemVerilog-2005 and VHDL-2008.
- The BluePrint Platform Designer for clock and I/O interface planning.
- The Rapid Recompile feature now supports Arria 10 devices.
- A hierarchical database infrastructure to enable faster and more scalable algorithms for next-generation programmable devices.
- Generation of Fitter reports upon completion of each Fitter compilation stage, providing earlier access to design compilation data.
- Ability to load post-plan and post-place timing netlists into the TimeQuest Timing Analyzer, for earlier analysis including Synopsys Design Constraints (SDC) verification and clock timing analysis.

Operating System Support

Information about OS support for the Quartus Prime Design Suite® is available on the Operating System Support page of the Altera website.

Related Information

Operating System Support

Memory Recommendations

A full installation of the Quartus Prime software requires up to 24 GB of available disk space.

Altera recommends that your system be configured to provide virtual memory equal to the recommended physical RAM that is required to process your design.

Note: Peak virtual memory may exceed these recommendations. These recommendations are based on the amount of physical memory required to achieve runtime within 10% of that achieved on hardware with an infinite amount of RAM.

Table 1: Memory Requirements for Processing Designs

These requirements are the same for both Windows and Linux installations.

Family	Device	Recommended Physical RAM
Arria 10	10AT115, 10AX115	48 GB
	10AX090	44 GB
	10AS066, 10AX066	32 GB
	10AS057, 10AX057	30 GB
	10AS048, 10AX048	28 GB
	10AX032, 10AS032	24 GB
	10AX027, 10AS027	22 GB
	10AX022, 10AS022	20 GB
	10AX016, 10AS016	18 GB

Changes in Device Support

Table 2: Device Support Fixed

Description	Workaround
EyeQ does not run without PRBS checker in Arria 10 designs The EyeQ **Start** button is grayed out when attempting to test a transceiver channel. This issue occurs when testing a transceiver channel without first associating either a hard or soft PRBS checker to that channel.	This issue is fixed in Quartus Prime software version 15.1

Related Information

Altera Knowledge Base
For more information about known device issues and workarounds.

Changes to Software Behavior

This section documents instances in which the behavior and default settings of the Quartus Prime Pro Edition software have been changed from earlier releases of the Quartus II software or from the Quartus Prime Standard Edition software.

Refer to the Quartus Prime Default Settings File (**.qdf**), ***<Quartus Prime installation directory>*/quartus/bin/assignment_defaults.qdf**, for a list of all the default assignment settings for the latest version of the Quartus Prime software.

The new database infrastructure in the Quartus Prime Pro Edition software is not compatible with databases from Quartus Prime Standard Edition software

Archive your project in the Quartus Prime Standard Edition software before you migrate a design to the Quartus Prime Pro Edition software. After you migrate a design to the Quartus Prime Pro Edition software, you will not be able to open it or compile it again in the Quartus Prime Standard Edition software.

Upgrade all IPs in your project in the Quartus Prime Pro Edition software even if you have already upgraded them to the Quartus Prime Standard Edition software version 15.1

Spectra-Q Synthesis enforces IEEE language rules

Spectra-Q Synthesis disallows some coding styles that are supported in the Quartus Prime Standard Edition software version 15.1 and in previous Quartus II software versions. Designs that compiled in previous versions of the Quartus II software might require HDL changes to match the standard IEEE language syntax supported in Quartus Prime Pro Edition software.

Incremental Compilation and Design Partitions are not supported in the Quartus Prime Pro Edition software

Delete partition assignments from your Quartus Settings File (**.qsf**) because partition assignments generate an error in the Quartus Prime Pro Edition software.

Convert LogicLock region assignments to LogicLock Plus region assignments in the Quartus Prime Pro Edition software

Delete LogicLock™ region assignments from the project's QSF assignments because LogicLock region assignments generate an error in the Quartus Prime Pro Edition software. Replace LogicLock region assignments with the equivalent LogicLock Plus region assignments.

The Quartus Prime Pro Edition software does not apply changes you make in .qsf or in the Assignment Editor until the next full compilation

The **.qsf** file is read only at the beginning of synthesis in the Quartus Prime Pro Edition software version 15.1. Therefore, the Quartus Prime Pro Edition software does not apply the changes you make in **.qsf** or in the Assignment Editor until the next full compilation. However, many compiler settings are stored in a supplementary file that is re-read before every compilation stage. As a result, most changes you make in the **Compiler Settings** dialog box will be applied immediately.

Note: You cannot add new SDC files via the TimeQuest GUI in the current release because doing so involves a QSF modification. As a workaround, you can source the new SDC file from one of the existing SDC files.

The default setting for synchronizer identification in the TimeQuest Timing Analyzer has changed

- For metastability analysis, the default setting for synchronizer identification (`SYNCHRONIZER_IDENTIFICATION`) has changed from `OFF` to `AUTO`.
- During static timing analysis, the TimeQuest Timing Analyzer automatically treats the project-wide synchronizer identification `OFF` setting as `AUTO`. You may apply the `OFF` setting to individual instances.
- TimeQuest Timing Analyzer's automatic synchronizer detection feature might report clock-crossing transfers between related clocks as synchronizers. To suppress the reporting of these clock-crossing transfers, set `SYNCHRONIZER_IDENTIFICATION` to `OFF` for the associated registers.

Note: The TimeQuest Timing Analyzer lists all the auto-detected synchronizers in the metastability report. However, the report only shows the calculated mean time between failures (MTBF) values for synchronizers that you specify using the `FORCED` or `FORCED IF ASYNCHRONOUS` setting. Otherwise, the MTBF values appear as Not Calculated.

Related Information

Migrating to Quartus Prime Pro Edition

For more information on how to migrate your design to Quartus Prime Pro Edition software.

Device Support and Pin-Out Status

The Arria 10 ordering part number (OPN) list has been updated for the Quartus Prime software version 15.1.

Table 3: Full Device Support

Full compilation, simulation, timing analysis, and programming support is now available for the new devices listed in this table.

Device Family	Devices
Arria 10	10AS066ES, 10AX066ES, 10AX115ES, 10AX115E2, 10AT115E2, 10AX115E3

Table 4: Advance Device Support

Compilation, simulation, and timing analysis support is provided for these devices. The Compiler generates pinout information for these devices in this release, but does not generate programming files.

Device Family	Devices
Arria 10	10AX016, 10AS016, 10AX022, 10AS022, 10AX027, 10AS027, 10AX032, 10AS032, 10AX048, 10AS048, 10AX057, 10AS057, 10AX066, 10AS066, 10AX090, 10AX115, 10AT115

Timing and Power Models

Table 5: Timing and Power Model Status

Device Family	Device	Timing Model Status	Power Model Status
Arria 10	10AX016, 10AS016, 10AX022, 10AS022, 10AX027, 10AS027, 10AX032, 10AS032,10AX048, 10AS048, 10AX057, 10AS057, 10AX066, 10AS066, 10AX090, 10AX115, 10AT115	Preliminary	Preliminary

Related Information

System Design with Advance FPGA Timing Models

IBIS Models

Table 6: IBIS Model Status for the Quartus Prime Pro Edition Software Release Version 15.1

Device Family	IBIS Model Status
Arria 10	Preliminary - 15.1

EDA Interface Information

Table 7: Synthesis Tools Supporting the Quartus Prime Pro Edition Software Release Version 15.1

Synthesis Tools(1)	Version	NativeLink Support
Mentor Graphics® Precision	2015a	No
Synopsys® Synplify, Synplify Pro, and Synplify Premier	2015.09	No

Table 8: Simulation Tools Supporting the Quartus Prime Pro Edition Software Release Version 15.1

Simulation Tools	Version	NativeLink Support	Gate-Level Simulation Support
Aldec Active-HDL	10.2 Update 2	No	Yes
Aldec Riviera-PRO	2015.06	No	Yes

(1) EDA Synthesis tools that support the Quartus Prime software version 15.1 will be released by vendors shortly after the release of the Quartus Prime software. Contact your vendor account manager for details.

Simulation Tools	Version	NativeLink Support	Gate-Level Simulation Support
Cadence Incisive Enterprise Simulator (IES)	14.2 (Linux only)	No	Yes
Mentor Graphics® ModelSim® PE	10.4b	No	Yes
Mentor Graphics ModelSim SE	10.4b	No	Yes
Mentor Graphics ModelSim-Altera	10.4b	No	Yes
Mentor Graphics Questa®	10.4b	No	Yes
Synopsys VCS and VCS MX	2014.12-SP1 (Linux only)	No	Yes

OS support for Mentor Graphics ModelSim-Altera version 10.4b (requires 32-bit libraries)

- Windows 7 SP1 (64-bit)
- Windows 8.0 (64-bit)
- Windows Server 2008 R2 SP1(64-bit)
- Red Hat Enterprise Linux 5.10 (64-bit)
- Red Hat Enterprise Linux 6.5 (64-bit)

Antivirus Verification

The Quartus Prime software release version 15.1 has been verified virus free using the following software:

Antivirus Verification Software for Windows

McAfee VirusScan Enterprise + AntiSpyware Enterprise Version: 8.8.0 (8.8.0.1445)
Scan Engine Version (32 bit): 5700.7163
Scan Engine Version (64 bit): 5700.7163
DAT Version: 7947.0000

Antivirus Verification Software for Linux

McAfee VirusScan Enterprise for Linux Version 1.9.1
Engine Version: 5700.7163
DAT Version: 7720

Known Issues and Workarounds

This section provides information about the following known issues that affect the Quartus Prime Pro Edition software version 15.1.

Description	Workaround
The Quartus Prime Pro Edition software version 15.1 does not support the following features: • FastForward Compilation • Back Annotation • NativeLink • OpenCore Plus • Video IP • Equation writing • Memory Initialization File update	These features will be supported in a future release of the Quartus Prime Pro Edition software.
For DSP Builder, floating-point designs targeting Arria 10 devices cause an internal error to occur in Mentor Graphics ModelSim Altera Edition version 10.4b.	Simulate your design using ModelSim Altera Edition version 10.3d or ModelSim SE version 10.4b.

When you regenerate the Altera I/O Phase-Locked Loop (Altera IOPLL) IP core in the Quartus Prime software, the name of a PLL in the netlist might change. As a result, the Quartus Prime software might ignore any Quartus Settings File (QSF) assignments or Synopsys Design Constraint (SDC) constraints containing the modified PLL name.
For example, the name of the PLL might change from
`u0|iopll_0|altera_pll_i|general[0].gpll~IOPLL`
to
`u0|iopll_0|altera_pll_i|twentynm_pll|iopll_inst`
	If your design contains any QSF assignments or SDC constraints that target I/O PLL nodes, check the names of the PLLs and make any necessary updates.
	In the Altera IOPLL IP parameter editor, ensure that you fill in the **Clock Name** field for the output clock. The PLL name change issue does not affect the SDC clock names produced by `derive_pll_clocks` as long as the **Clock Name** field is not blank.
	Altera recommends checking the clock names to make sure they remain consistent when you migrate your design to the Quartus Prime software version 15.1.

Because of the hierarchical manner in which the Quartus Prime Pro Edition software organizes the design database files, an internal error might occur in the Windows version of the Quartus Prime Pro Edition software when the file path to a design file is too long.	Windows has a 260-character limit on the combined length of a file name and its file path. To reduce the length of a file path to a design file, avoid storing your Quartus Prime project in a directory that is far removed from the drive location.
The Altera In-System Sources and Probes hardware component description file (**altera_in_system_sources_probes_hw.tcl**) does not support VHDL generation in the Quartus Prime Pro Edition software.	Generate the system in Verilog.

Description	Workaround
If you invoke BluePrint's Autoplace All feature to place the periphery for the following designs, BluePrint generates assignments that might cause an internal error in Spectra-Q Synthesis (`quartus_syn`) when they are added to the Quartus Prime Settings File (**.qsf**): • Designs that have the SignalTap™ II Logic Analyzer Trigger out to pin feature, or both, enabled. • Designs that contain the Arria 10 Transceiver Native PHY IP core with the `tx_analog_reset` or `rx_analog_reset` signal connected to the top-level inputs.	If your designs satisfy the listed criteria, avoid using BluePrint's AutoPlace All feature. Alternatively, remove the assignments that cause the internal error in `quartus_syn`. These assignments have targets to hierarchy paths of the form `auto_fab_0|debug.export.*`. For example: `set_location_assignment IOOBUF_X142_Y44_N18 -to auto_fab_0|debug.export.alt_sld_fab_0_splitter_receive_1[0]~output -tag "BluePrint Location Assignment"`
The I/O pad atom does not replace the logical pin name. Instead, the I/O pad atom is inserted in between the logical pin name and the rest of the logic, and it is given a suffix of `~pad`. However, all assignments made to the logical pin name, including location constraints, are automatically applied to the pad. For example, for a logical pin named `clk`, the corresponding pad is called `clk~pad`. If you have a location assignment to `clk`, the assignment is applied to `clk~pad` instead of `clk`.	This issue will be fixed in a future release of the Quartus Prime Pro Edition software.
Including Altera-specific directives, such as `(* preserve*)` and `(* keep*)`, in a source file that is used on large buses or in frequently-instantiated modules might degrade performance.	Remove the Altera-specific directive and create the corresponding setting in the design's **.qsf** file. For example, instead of writing `(* preserve*) [N:0] abc` in module `def`, add the following setting in the **.qsf** file: `set_instance_assignment -name PRESERVE_REGISTER ON -entity def -to abc`

Latest Known Quartus Prime Software Issues

Information about known software issues is available on the Quartus Prime Software Support webpage.

You can find known issue information for previous versions of the Quartus II software on the Altera Knowledge Database webpage.

Information about issues affecting the Altera IP Library is available in the *Altera IP Release Notes*.

Related Information

- **Quartus Prime Software Support**
- **Altera Knowledge Database**
- **Altera IP Release Notes**

Document Revision History

Table 9: Quartus Prime Software Release Version 15.1 Document Revision History

Date	Version	Changes
November 2015	15.1.0	Initial release.