Product Brief

FPGAs and SoCs

Intel Agilex® 7 FPGA Accelerators Bring Improved TCO, Performance, and Flexibility to 4th Gen Intel® Xeon® Platforms

Highlights

- Intel is the volume leader in the Infrastructure Processing Unit (IPU) market working with many leading providers and majority of Tier 1 Cloud Service Providers
- The industry's first FPGA with dedicated Compute Express Link (CXL) intellectual property (IP) block, providing 4X higher CXL bandwidth per port vs. other FPGA CXL implementations[1]

Top five reasons to use discrete Intel FPGA accelerators

- Lower TCO
- Increased system flexibility
- Differentiation
- High performance
- Increased security

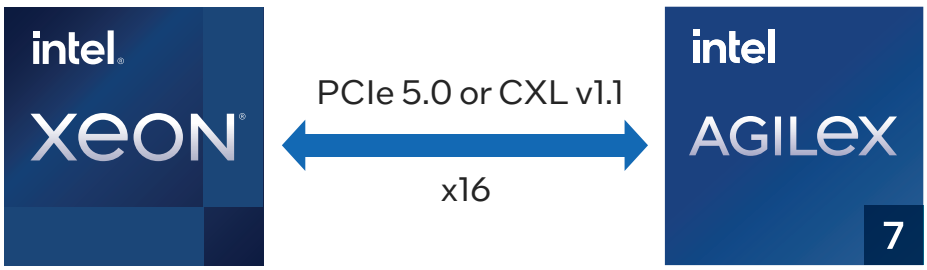
The relentless demands of emerging workloads for performance and the phenomenal growth of data flowing into data centers and networks are driving the need for faster processing and more memory bandwidth. Accelerators help speed up complex tasks and improve overall efficiency, lowering total cost of ownership. 4th Gen Intel® Xeon® Scalable processors are designed to accelerate performance across the fastest-growing workloads and have the most built-in accelerators of any CPU on the market to improve performance in artificial intelligence (AI), analytics, networking, storage, and HPC.

Intel FPGAs as Discrete Accelerators

Use of accelerators alongside newer and faster CPUs is growing rapidly as a common server architecture. Pairing 4th Gen Intel Xeon processors with Intel Agilex 7 FPGA-based accelerators can improve the total cost of ownership (TCO) of a server and increase data center utilization by freeing up CPU cores used on infrastructure or microservices so those cores can be re-used on other high value tasks – improving compute efficiency so customers can run additional workloads without new server investment.

FPGAs can be reprogrammed to match specific workloads for a variety of applications, helping customers manage and thrive in an environment marked by constant change. This flexibility allows changes to be made throughout the lifecycle of the system, from bug fixes during prototyping to adding new features to systems already deployed in the field. Hardware programmability also allows equipment providers the ability to quickly differentiate their product versus the competition by adding in new and unique features. FPGAs are well known as devices with the fastest time to market for implementing new features and getting them to market.

By offloading selected algorithms from the CPU to FPGA hardware (ie hardware vs software execution), greater performance can be achieved by using parallel processing techniques. Intel Agilex 7 FPGA accelerators also provide system-wide performance benefits utilizing the high throughput, scalable IO technologies of PCIe 5.0 and Compute Express Link (CXL) in the new 4th Gen Intel Xeon based servers.



Customer Benefits Based on 3rd Party Testing [2,3,4,5]

Check out some examples of early customer results when using Intel Agilex 7 FPGAs with 4th Gen Intel Xeon Scalable processors:

- Meta (Cloud) – Adding CXL memory to 4th Gen Intel Xeon-based servers and using Transparent Page Placement memory algorithms improves Linux performance up to 18% for cloud-based workloads. This results in TCO savings as CXL allows more efficient use of server memory.
- Unifabrix (HPC) – Adding CXL memory to 4th Gen Intel Xeon-based server increased the HPCG score by 26% and increased CPU cores used by 189%.
- Liquid Markets (FSI) – Using CXL, achieves a 30% reduction in latency for various Electronic Trading workloads. Time is money and leveraging Intel Agilex 7 FPGAs with CXL results in faster execution of financial models.
- Atomic Rules (General Compute)– Atomic Rules' Arkville data mover IP implemented within Intel Agilex 7 FPGAs results in up to 400 Gbps PCIe 5.0 throughput. For applications requiring high data transfer with low latency between host memory and FPGA, this solution minimizes CPU core usage and eliminates memory copies, thus improving overall system efficiency.

Intel Agilex 7 FPGAs offer several security features, which can be combined with system designer created unique algorithms (like an improved encryption/decryption function) to add another layer of security for the overall system. For those who use the FPGA accelerator to offload infrastructure or microservices from the CPU to the FPGA, a security 'airgap' is created which allows for application and tenant isolation between the offloaded work on the FPGA and the rest of the CPU operations.

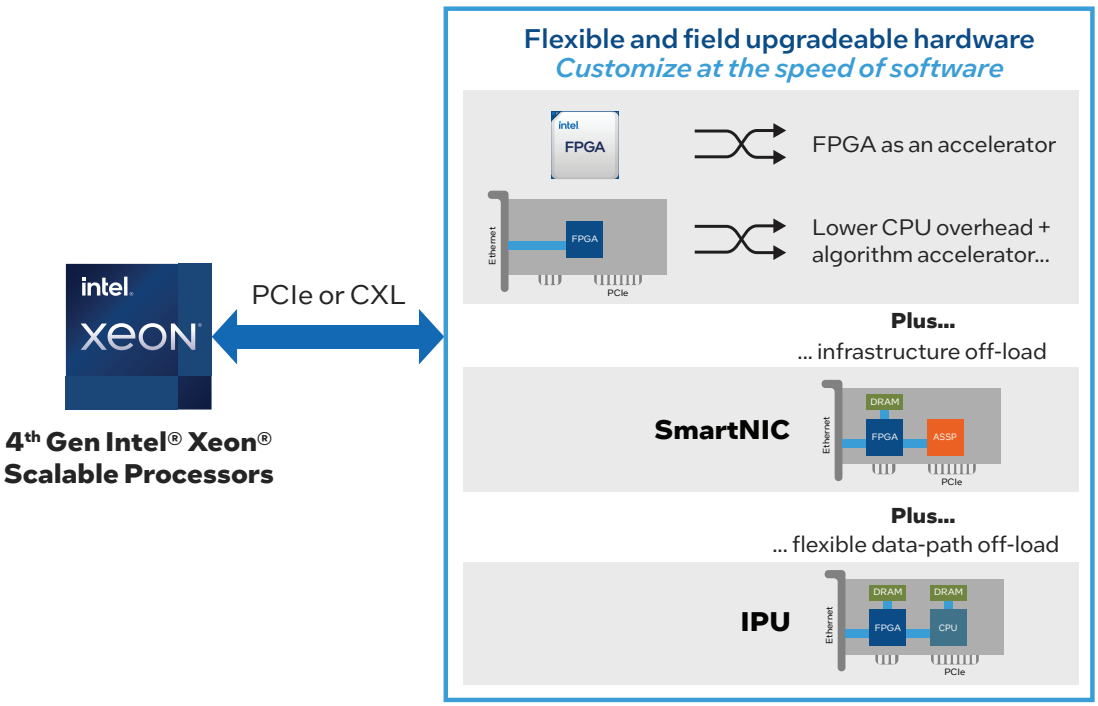
Create Custom Solutions with Open FPGA Stack

Intel Agilex 7 FPGA-based accelerators allow you to create unique acceleration platform solutions using the new Open FPGA Stack (OFS). Delivered via git repositories, this scalable infrastructure can accelerate software, hardware, and workload development for a wide range of projects. Use this new framework to create custom platform solutions using source-accessible OFS hardware and software code. Customers using this new framework have already experienced faster time to deployment thanks to upstreamed OFS kernel and user space code. FPGA support for other acceleration related software include oneAPI, Data Plane Development Kit (DPDK), Infrastructure Programmer Development Kit (IPDK), P4, and more.

Intel Agilex 7 FPGAs: An Ideal Building Block for Discrete Accelerators

The Intel Agilex 7 FPGA family leverages the full breadth of Intel innovation, manufacturing capability, and supply resiliency. Built with advanced 10 nm SuperFin technology (F-Series and I-Series), Intel 7 technology (M-Series), and a second-generation Intel® Hyperflex™ FPGA Architecture, Intel Agilex 7 devices deliver ~2X better fabric performance per watt[6] compared to competing 7 nm FPGAs. Intel Agilex 7 devices also offer integrated Arm-based processors, support for DDR5 and HBM2e, transceivers up to 116Gbps, 400GbE, hardened high-speed cryptographic engines paired with MACsec IP, PCI Express (PCIe) 5.0, and CXL (v1.1 and v2.0).

Together, Intel Agilex 7 FPGAs with 4th Gen Intel Xeon Scalable processors provide server platforms with the ultimate combination of computing capability and accelerators for addressing a wide variety of workloads and use-cases.



Customer success

Meta Leverages CXL to Increase Utilization of Cloud Server Memory Resources

- Read the white paper: https://arxiv.org/abs/2206.02878
- Watch the CXL demo video: https://www.youtube.com/watch?v=IswQCyHnauY

Target Applications

Platforms	Description	Target Applications
IPU Platforms and Adapters 	• Advanced networking device with hardened accelerators and Ethernet connectivity • Accelerates and manages infrastructure functions using tighly coupled, dedicated, programmable cores. • Offers full infrastructure offload and provides an extra layer of security by serving as a control point of the host for running infrastructure applications.	Cloud infrastructure workloads such as: • Open vSwitch • NVMe over Fabrics • Remote Direct Memory Access (RDMA over Converged Ethernet v2 (RoCEv2))
SmartNICs 	• Programmable network adapter card with programmable accelerators and Ethernet connectivity. • Accelerate infrastructure applications running on the host CPU.	• Internet Protocal Security (IPSec) • vFirewall • Segment Routing Version (SRv6) • Virtual Network Functions (vNFs) • Professional Media over Managed IP Networks • 4G/5G Virtualized Radio Access Networks (vRAN)

For more details on Intel FPGA acceleration boards and platforms, go to https://www.intel.com/content/www/us/en/products/details/fpga/platforms.html

Learn More

www.intel.com/AccelerateWithXeon

www.intel.com/agilex

Footnote 1 – Intel estimates based on Intel Agilex 7 FPGA CXL hard + soft IP test results (CXL link at Gen5 x16) versus Xilinx FPGA using 3rd party CXL soft IP (CXL link at Gen4x8), both interop with pre-production 4th Gen Intel Xeon processors.

Footnote 2 – Source: https://arxiv.org/abs/2206.02878. Based on 3rd party implementation & benchmark using pre-production 4th Gen Intel Xeon processors, Intel Agilex 7 FPGAs, and Intel FPGA CXL IP. Results may vary.

Footnote 3 – Based on 3rd party implementation and benchmark using pre-production 4th Gen Intel Xeon processors, Intel Agilex 7 FPGAs, and Intel FPGA CXL IP.

Footnote 4 – Source: https://www.businesswire.com/news/home/20221018005068/en/Liquid-Markets-Unveils-%C3%9CberNIC%E2%84%A2-an-Ethernet-Adapter-Exclusively-Based-on-Intel-Agilex-FPGAs. Based on 3rd party implementation & benchmarks. Results may vary.

Footnote 5 – Based on 3rd party implementation and benchmark using pre-production 4th Gen Intel Xeon processors, Intel Agilex 7 FPGAs, and Intel FPGA PCIe 5.0 IP. Results may vary.

Footnote 6 – Performance varies by use, configuration and other factors. Learn more at www.intel.com/PerformanceIndex (see the FPGA section for specific workloads and configurations). Results may vary.

Intel does not control or audit third-party data. You should consult other sources to evaluate accuracy.

SB- 01155-1.1