Intel® Socket Test Technology

Application Note for the LGA771 Product Code JM8FKZLVA

February 2006

Document Number: 311708-001

Notice: This document contains information on products in the design phase of development. The information here is subject to change without notice. Do not finalize a design with this information.

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Revision History

Reference Number	Revision Number	Description	Date
311708	-001	• Initial release of the document.	February 2006

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1 Introduction

The Intel® Socket Test Technology for the LGA771 socket is a test chip that enables testing for the mechanical integrity and electrical continuity of both socket-to-board solder ball connectivity and socket-to-CPU contact connectivity. Once inserted into the board's LGA771 socket, the test chip works with either in-circuit testers (ICT) or manufacturing defect analyzers (MDA) that have access to all the socket nets through test fixture probes.

An ICT uses digital test vectors which execute very quickly when power is applied to the board—typically less than a couple of milliseconds depending upon test head capability. An MDA doesn't power the board, but uses its analog measurement capability. Test time using an MDA is typically longer.

Figure 1-1. Intel® Socket Test Technology for the LGA771 Socket-Test Chip JM8FKZLVA

1.1 Terminology

Table 1-1. Terms and Descriptions

Term	Description
ICT	In-circuit Test
LGA771 socket	Processor in the 771-land package mates with the system board through a surface mount, 771-pin, LGA (Land Grid Array) socket.
MDA	Manufacturing Defect Analyzer
VCCP	Processor core voltage
VTT	IO termination voltage for the front side bus

1.2 Reference Documents

Table 1-2. Reference Documents

Documents	Notes
TBD	1

NOTE: This section will be updated in the next version.

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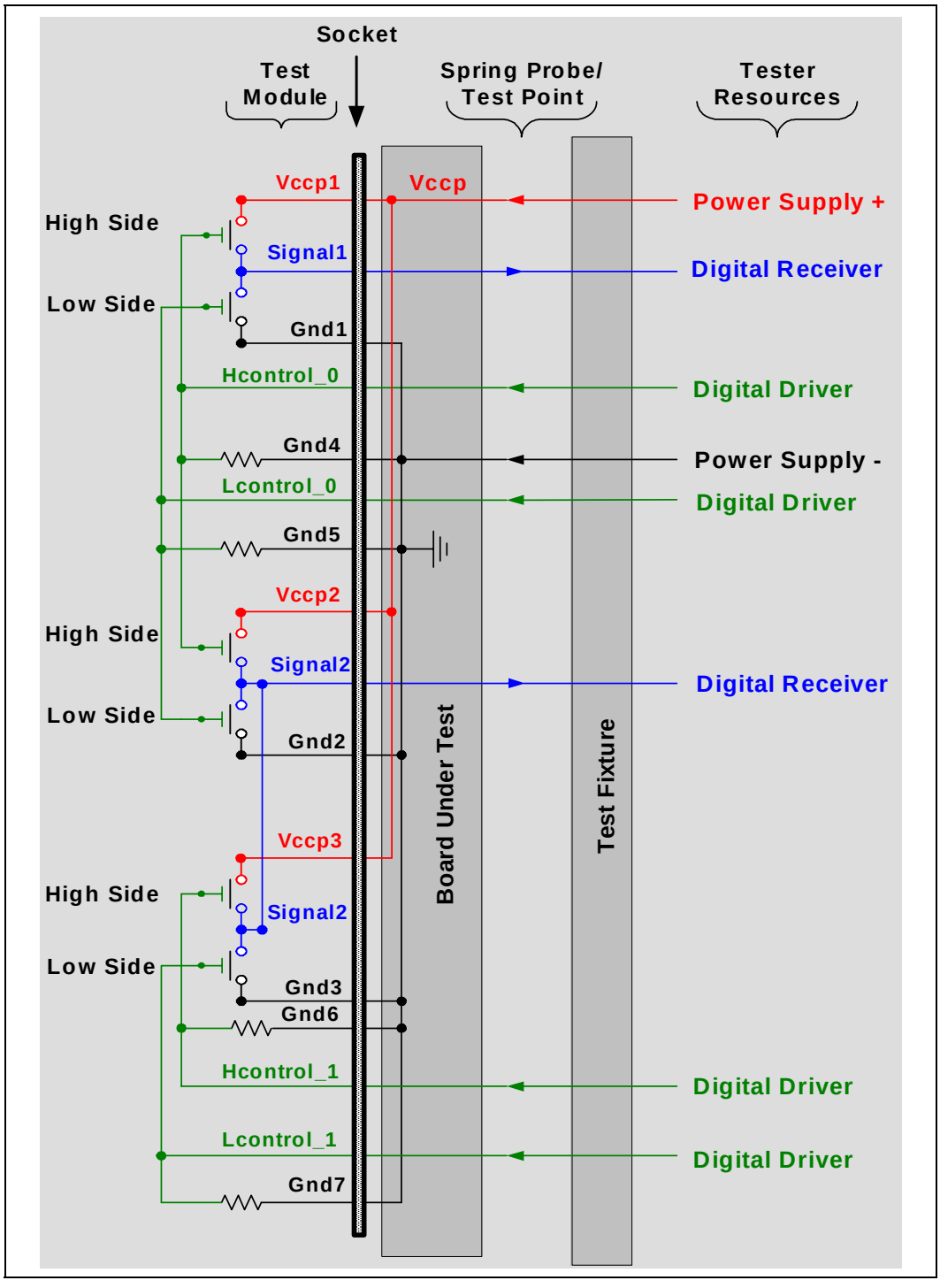
2 Theory

The Intel® Socket Test Technology LGA771 socket test chip consists of an array of switch pairs. Each switch pair, together with a control signal, can be used to test one signal, one power, and one ground. The control signal enables the **ON**/**OFF** condition of each switch. Testing is accomplished by checking the **ON** and **OFF** condition of each switch. There are fewer signals than power and ground electrical socket connections. To compensate there are four pairs of Hcontrol and Lcontrol signals that allow the multiplexing of signals between power and ground electrical socket connections. Signal multiplexing provides testing for as many power and grounds as possible. Testing of resistors that are also on the test chip help to provide some additional open coverage not provided by the switch pairs.

The control signals are pulled to ground with a resistor to keep the switches in an **OFF** state when a powered test method is being used on an ICT.

Figure 2-1. Intel® Socket Test Technology for the LGA771 Socket-Bock Diagram



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3 Powered Testing With Digital Vectors (ICT)

3.1 Using Voltage Identifier (VID) Signals

VCCP and VTT are used to power the test chip. The test chip does not provide control on the VID signals to establish a VCCP voltage when plugged into a socket. **A VID signal combination should be connected to ground and controlled by the test equipment in such a way that an on-board VCCP is generated that equals the on-board VTT voltage.**

To determine which VID lines to use in order to keep VCCP equal to VTT, refer to the Voltage Regulator Down (VRD) Design Guide for the processor being used (Section 1.2 of this document).

Table 3-1. Voltage Identifier Signals

Signal Name	VID Ball
VID_0	AM2
VID_1	AL5
VID_2	AM3
VID_3	AL6
VID_4	AK4
VID_5	AL4

3.2 Using Control Signals

To ensure that the switches default to **OFF** when power is applied or while other devices are being tested, the control signals are pulled to ground with 1 k resistors. Each control signal can turn a grouping of approximately 128 switches **ON** and **OFF**.

Each **ON**/**OFF** switch pair tests three socket solder balls and socket contacts, not including the control signals. A logic level high on the control signal will turn its associated switch to the **ON** state.

Two pairs of Hcontrol and Lcontrol inputs are used to multiplex the signals that are received by the test equipment across more than one switch pair in order to test the majority of power and ground electrical socket connections.

Caution: **X** - At no time should the control signal for the *High Side* and *Low Side* switches be driven high at the same time, as occurs with some automated fault injection tools. A direct short from power to ground would result and possibly damage the Intel® Socket Test Technology test chip and the

board under test. To prevent damage, drive only one control signal high at any time during the test while all others are low.

The High Side switch of each switch pair is used to test a VCCP solder ball and contact along with the shared signal solder ball and contact of the High and Low Side switch pair. The control line for the High Side switch is driven to a logic high, thus turning the switch **ON** and enabling an electrical connection between VCCP and the shared signal. When this happens, a logic high should be received on the shared signal. At the same time, the Low Side switch control signal will be at a logic low.

The Low Side switch of each switch pair is used to test a GND solder ball and contact along with the shared signal solder ball and contact of the High and Low Side switch pair. The control line for the Low Side switch is driven to a logic high, thus turning the switch **ON** and enabling an electrical connection between GND and the shared signal. A logic low should be received on the shared signal. At the same time, the High Side switch control signal will be at a logic low.

One shared signal is used to test one VCCP and one GND connection. The lack of the high/low signal transition would indicate an open on either the shared signal or the power/ground connection used by that switch pair.

Table 3-2 shows that **Signal1**, **Vccp1**, and **Gnd1** as well as **Signal2**, **Vccp2**, and **Gnd2** can be verified through **Hcontrol_0** and **Lcontrol_0**.

Table 3-2. Control Signals

Signal Name	Signal Ball
Hcontrol_0	E5
Lcontrol_0	E6
Hcontrol_1	D1
Lcontrol_1	D14

As with all powered digital in-circuit testing, all other active components on the board that are connected to the socket should be placed in a tri-state mode before testing with this technique.

3.3 Using Test Head Loads

Test head loads (pull-ups/pull-downs) improve the detection of opens. With the switch pair **OFF**, the signals would be pulled to a logic level low if test head pull-downs are used and a logic level high if test head pull-ups are used. Using pull-ups with the Low Side switch **ON** would receive a logic level high on the signal if the signal or GND connection were open and a logic level low if they were not open. Using pull-downs with the High Side switch **ON** would receive a logic level low on the signal if the signal or VCCP ball were open and a logic level high if they were not open. Note: On-board pull-up/down resistors must be taken into consideration when test head loads are used.

Table 3-3. Sample Table

Inputs			Output Signal
Low Side Control	High Side Control	Test Head Load	
0	0	Pull-Down	0
0	0	Pull-Up	1
1	0	Pull-Up	0
0	1	Pull-Down	1
1	1	N/A	X

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4 Un-Powered Testing (MDA)

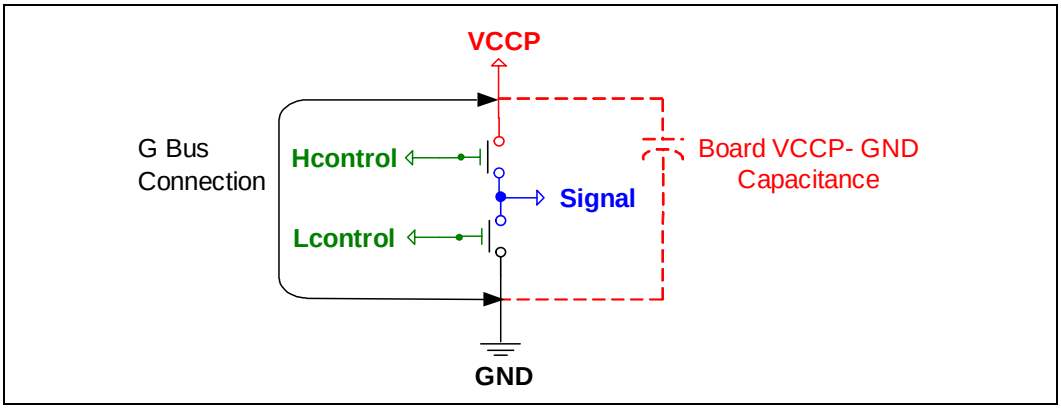
The following test method was developed using an Agilent* 3070 Series II In-circuit tester in an un-powered mode. The technique and results should be similar when using test equipment with similar capabilities as described below. (Please note that Agilent was formerly known as Hewlett Packard* or HP).

Table 4-1. Test Equipment Technique

Bus	Description
S Bus	Primary Source. Provides -10.0V to +10.0V (VDC) by connecting the high side to the Device under Test (DUT) through a 500 series resistance. The low side connects itself automatically to digital and switched analog GND.
A Bus	Auxiliary Source. Provides -10.0V to +10.0V (VDC) by connecting the high side to the DUT and the low side automatically to digital and switched analog GND.
I Bus	The high side of a DC voltmeter connected to the DUT.
L Bus	The low side of a DC voltmeter connected to digital and switched analog GND unless otherwise specified through software.
G Bus	Guard Bus. Used to break parallel impedance paths. In this case, it connects VCCP and GND to keep them at the same potential.

The typical Intel® Socket Test Technology switch pair is shown in Figure 4-1 using the G Bus to short circuit VCCP to GND and potentially eliminates the charge/discharge time caused by the large capacitance present on the board when testing the High Side switch. The intent is to make the over all test as fast and reliable as possible.

Figure 4-1. Typical Switch Pair Configuration



Each switch is tested by connecting the A Bus to the Hcontrol or Lcontrol, the S and I Buses to the Signal, and the L Bus to GND. The A Bus is set to 1.2V to ensure a positive turn on of the switch. The S Bus is set to 600mV for the High and Low Side switch. The S Bus uses a 500 series resistance for both the High and Low Side switch.

The resistance of the switch is equal to approximately 40 in the **ON** state and is infinite in the **OFF** state. In an isolated environment, the **ON** state voltage measured at the signal would be approximately 44mV as a voltage divider exists between the 40 switch resistance and the 500 resistance of the source termination.

It has been observed that the **OFF** state voltage doesn't reach the 600mV level that circuit theory would lead one to expect. This is due to the influence of other on-board devices that cause the level to settle at approximately 250mV.

Figure 4-2. Instrument Setup For Low Side Switch

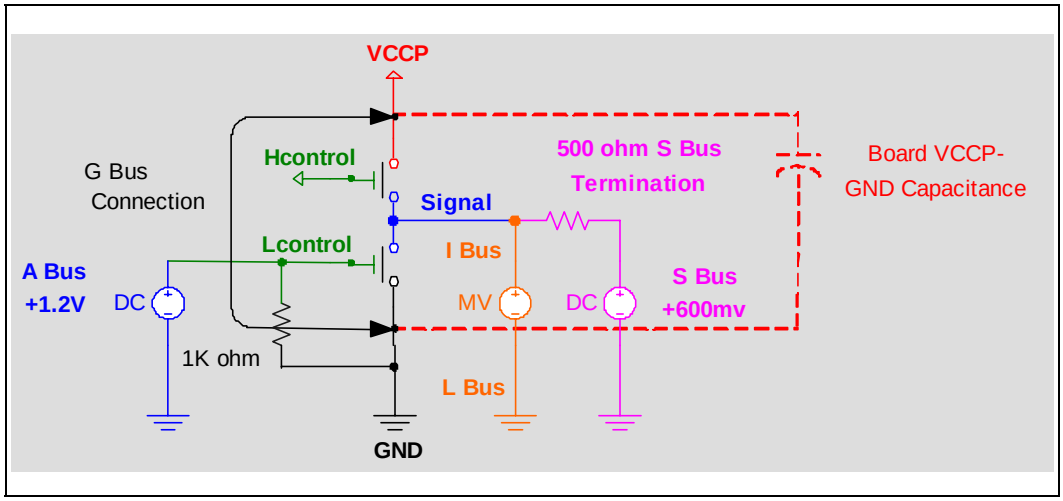
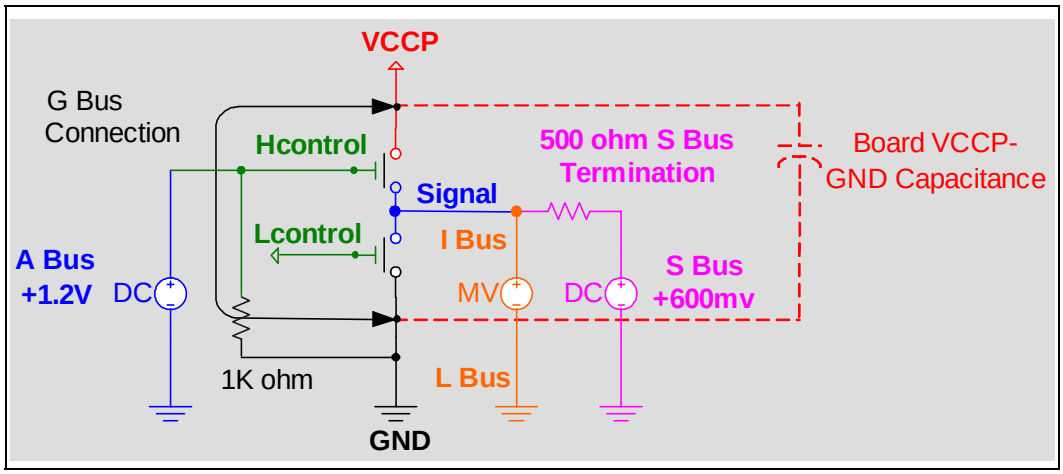


Figure 4-3. Instrument Setup For High Side Switch



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5 Board Design Impact on Test Results

After the production of Intel® Socket Test Technology for LGA771 had begun, changes were made to board design around the processor socket that will impact test results. These changes affect four pins—A24, E29, G1, and U1—that were connected to the VSS (Ground) plane in the original board design. The pins are still in the GND column of the Ball Usage tables in Section 7, but they have been high-lighted in grey to call attention to the change.

Since the change affects particular boards, it is recommended that each design be reviewed to determine if any or all of these pins are used as signals or VSS.

5.1 How to Test

If the pins are used as signals rather than ground or power, possible techniques to keep test results the same include the following:

- Place test points on the pin nets and use fixture relays to connect the pins to VSS prior to powering up the board or testing the socket using the un-powered test method. Fixture relays that can be activated and deactivated through program control will accommodate the “Shorts” test.
- Use test points and test head resources to put the pins at a VSS level while using the powered or un-powered test methods.

5.2 U1 Pin for Powered Testing

If U1 is a signal rather than ground, and the board under test is to be powered up, then the board design **must** include a test point on the board net for the U1 pin. In the original design, U1 was the ground path for control pin E5. It was used to ensure that the switches defaulted to the OFF state when power was applied or while other devices were being tested.

In designs where U1 is a signal pin, it should be tied to VSS (Ground) through fixture relays that can be activated and deactivated through program control to accommodate the “Shorts” test. To ensure that the switches default to **OFF** when power is applied or while other devices are being tested, the control signals are pulled to ground with 1k resistors.

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6 Related Specifications

Operating temperature: Between 10° C and 50° C

Electrostatic Discharge (ESD) Environment: Controlled to less than 300 volts

Table 6-1. Electrical Operating Parameters

Symbol	Parameter	Value	Units
Vccp	Applied Voltage (Powered)	0.8 to 1.2 max	V
CtrlOnThres	Switch On Threshold	300	mV
HctrlEnVih	High Switch Enable VIH (Powered)	Vccp + 0.6 max	V
LctrlEnVih	Low Switch Enable VIH (Powered)	Vccp + 0.6 max	V
CtrlDisVil	Switch Disable VIL	0.0	V
CtrlEnVih	Switch Enable Voltage (Un-powered)	1.2 max	V
Sd(on)	Switch Control On To Signal Out Delay (Powered)	20	us
Sd(off)	Switch Control Off To Signal Out Delay (Powered)	20	us
Rval	Resistor Value (Un-Powered)	1k(+-5%)	Ω
RvalControl	Resistor Value of Four Control Signals (Un-Powered)	1k(+5%, -40%)	Ω
Hid(on)	High Switch On Saturation Current	20	mA
Lid(on)	Low Switch On Saturation Current	26	mA

Table 6-2. Test Condition for High Side Switch (Powered Digital)

Symbol	Parameter	Value	Units
Vccp	Applied Voltage	1.2 max	V
Hcontrol	Enable High Side Switch	1.8 max	V
Lcontrol	Disable Low Side Switch	0.0	V
Signal	Minimum VOH	600	mV
Signal Load	Current Source from Signal to Ground (Pull Down)	5	mA
Signal VohTh	Test VOH Threshold Setting	400	mV
Signal VolTh	Test VOL Threshold Setting	400	mV

Table 6-3. Test Condition for Low Side Switch (Powered Digital)

Symbol	Parameter	Value	Units
Vccp	Applied Voltage	1.2 max	V
Hcontrol	Disable High Side Switch	0.0	V
Lcontrol	Enable Low Side Switch	1.8 max	V
Signal	Maximum VOL	200	mV
Signal Load	Current Source from Signal to Vccp (Pull Up)	2	mA
Signal VohTh	Test VOH Threshold Setting	400	mV
Signal VolTh	Test VOL Threshold Setting	400	mV

Table 6-4. Test Condition for Switch (Un-powered Analog)

Symbol	Parameter	Value	Units
VccpToGnd	Vccp Connected To Gnd	0.0	V
HctrlEn	Enable High Side Switch	1.2 max	V
HctrlDis	Disable High Side Switch	0.0	V
LctrlEn	Enable Low Side Switch	1.2 max	V
LctrlDis	Disable Low Side Switch	0.0	V
SigSrcVolt	Signal Applied Source Voltage	600 max	mV
SigSrcVR	Signal Applied Source Voltage Resistance	500	Ω

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7 Ball Usage

Table 7-1 identifies the balls used for the 4 control lines, also referred to as Lcontrol_0 – Lcontrol_1 and Hcontrol_0 – Hcontrol_1.

Table 7-1. Balls Used as Control Signals

Low Side Control (Lcontrol)	High Side Control (Hcontrol)
E6	E5
D14	D1

Table 7-2 maps the ball of the *High* and *Low Side* controls with the signal ball, ground ball and power ball for each switch pair. The table can be used to generate tests and diagnose test failures.

Table 7-2. Ball Groupings/Functions

Low Side Control	High Side Control	Signal	GND	VCCP
E6	E5	G16	H27	T27
E6	E5	G17	L30	T28
E6	E5	F15	AE24	T29
E6	E5	G15	H26	T26
E6	E5	G14	H24	T24
E6	E5	F17	H25	T23
E6	E5	E15	AF30	T30
E6	E5	F14	H23	U30
E6	E5	G18	H21	U29
E6	E5	E16	H22	U28
E6	E5	E18	AF29	N23
E6	E5	F18	H19	N24
E6	E5	E13	E28	U27
E6	E5	G13	H20	N25
E6	E5	D17	AF28	N26
E6	E5	D13	E29	N27
E6	E5	E19	D24	N29
E6	E5	G19	E26	N28
E6	E5	E12	AF27	M23
E6	E5	D19	E25	N30
E6	E5	G12	A24	M25
E6	E5	F12	C24	M24
E6	E5	F11	AF26	M27

Table 7-2. Ball Groupings/Functions

E6	E5	G11	B24	M26
E6	E5	G20	D21	M29
E6	E5	D11	F22	M28
E6	E5	D20	E20	K23
E6	E5	F20	A21	M30
E6	E5	E10	AF25	K25
E6	E5	C20	B20	K24
E6	E5	F21	C19	K27
E6	E5	D10	F19	K26
E6	E5	G22	AJ30	K29
E6	E5	G21	D18	K28
E6	E5	C18	B17	J30
E6	E5	B19	A18	K30
E6	E5	C15	C16	J28
E6	E5	C17	F16	J29
E6	E5	C12	A15	J26
E6	E5	C14	D15	J27
E6	E5	B9	C13	J24
E6	E5	C11	E14	J25
E6	E5	F9	F13	J22
E6	E5	E9	B14	J23
E6	E5	E21	D12	J20
E6	E5	G9	A12	J21
E6	E5	B21	E11	J18
E6	E5	C21	B11	J19
E6	E5	B16	D9	C27
E6	E5	B18	C10	C25
E6	E5	B12	B8	C30
E6	E5	B15	A9	C29
E6	E5	A19	C7	B26
E6	E5	B10	F10	B25
E6	E5	A16	A6	B28
E6	E5	A17	D6	B27
E6	E5	A11	F4	B30
E6	E5	A14	B5	B29
E6	E5	A8	D3	A26
E6	E5	A10	C4	A25
E6	E5	F8	A2	D27
E6	E5	G8	E2	C26
E6	E5	C8	G1	F30

Table 7-2. Ball Groupings/Functions

E6	E5	D8	B1	E30
E6	E5	U6	Y7	V8
E6	E5	R6	AA6	AH19
E6	E5	P6	AA3	W8
E6	E5	T5	W7	AJ19
E6	E5	U5	Y5	Y8
E6	E5	V5	Y2	AK19
E6	E5	U4	AE17	AH22
E6	E5	T4	AN17	AG22
E6	E5	R4	W4	AA8
E6	E5	V4	V7	AL19
E6	E5	M4	V6	AB8
E6	E5	M5	V3	AM19
E6	E5	M6	AJ20	AF22
E6	E5	W5	AG23	AE21
E6	E5	W6	U7	AC8
E6	E5	P3	AH23	AE22
E6	E5	M3	T6	AG19
E6	E5	L4	T7	U8
E6	E5	L5	AH20	AN21
E6	E5	Y4	AJ23	AN22
E6	E5	Y6	R2	AF19
E6	E5	P2	AK23	AE23
E6	E5	N2	AG20	AE19
E6	E5	U2	AK24	AK25
E6	E5	K3	P7	P8
E6	E5	K4	R7	T8
E6	E5	K6	P4	R8
E6	E5	AA4	AJ24	AJ25
E6	E5	AA5	N6	N8
E6	E5	AB4	N3	AM21
E6	E5	AB5	AF20	AM22
E6	E5	AB6	AH24	AH25
E6	E5	J5	N7	AL22
E6	E5	J6	AG24	AG25
E6	E5	AC5	M7	L8
E6	E5	AD5	M1	M8
E6	E5	AD6	AE20	AF21
E6	E5	J17	AF24	AJ26
E6	E5	F5	L3	AG21

Table 7-2. Ball Groupings/Functions

E6	E5	L1	AL24	AK26
E6	E5	K1	L7	J10
E6	E5	U3	L6	K8
E6	E5	E3	AL20	AH21
E6	E5	E4	AL23	AL25
E6	E5	AF4	K2	AJ21
E6	E5	AF5	AM24	AL26
E6	E5	D2	K5	J11
E6	E5	D4	K7	AJ22
E6	E5	C1	AM23	AN25
E6	E5	C2	AN24	AM26
E6	E5	C3	H3	AK21
E6	E5	C5	J4	J12
E6	E5	C6	AM20	AM25
E6	E5	B2	J7	J13
E6	E5	G7	AN23	AL21
E6	E5	B3	AN20	AN26
E6	E5	B6	H6	AK22
E6	E5	B4	H7	AG26
E6	E5	A4	H8	J15
E6	E5	A3	AF23	AG27
E6	E5	D7	H10	AH27
E6	E5	A5	H9	J14
E6	E5	A7	H12	J9
E6	E5	B7	H11	J8
D14	D1	U6	AN17	AN14
D14	D1	R6	AB1	V8
D14	D1	P6	AN16	Y8
D14	D1	T5	AA7	W8
D14	D1	U5	AC3	AB8
D14	D1	V5	AB7	AA8
D14	D1	U4	AC7	AL8
D14	D1	T4	AC6	AC8
D14	D1	R4	AM17	AD8
D14	D1	V4	AM16	AN15
D14	D1	M4	AD4	AN9
D14	D1	M5	AD7	AM9
D14	D1	M6	AL17	AM15
D14	D1	W5	AE2	AL9
D14	D1	W6	AE16	AN11

Table 7-2. Ball Groupings/Functions

D14	D1	P3	AF3	AJ9
D14	D1	M3	AE7	AE9
D14	D1	L4	AE5	AK9
D14	D1	L5	AF7	AL11
D14	D1	Y4	AF6	AM11
D14	D1	Y6	AH1	AF11
D14	D1	P2	AG7	AK11
D14	D1	N2	AG17	AG11
D14	D1	U2	AF17	AM14
D14	D1	K3	AH3	AJ11
D14	D1	K4	AH6	AH11
D14	D1	K6	AH17	AL15
D14	D1	AA4	AH7	AE11
D14	D1	AA5	AJ4	AM12
D14	D1	AB4	AJ7	AN12
D14	D1	AB5	AL16	AK12
D14	D1	AB6	AK2	AL12
D14	D1	J5	AL3	AH12
D14	D1	J6	AK7	AJ12
D14	D1	AC5	AK17	AF12
D14	D1	AD5	AJ17	AL14
D14	D1	AD6	AE10	AE12
D14	D1	J17	AL7	AG12
D14	D1	F5	AF10	AJ14
D14	D1	L1	AG10	AH14
D14	D1	K1	AK16	AK14
D14	D1	U3	AH10	AG14
D14	D1	E3	AL10	AE18
D14	D1	E4	AJ10	AF14
D14	D1	AF4	AF16	AH18
D14	D1	AF5	AK10	AF18
D14	D1	D2	AM1	AJ18
D14	D1	D4	AM7	AG18
D14	D1	C1	AG16	AE15
D14	D1	C2	AN1	AH19
D14	D1	C3	AH16	AK19
D14	D1	G7	AM10	AL19
D14	D1	C5	AN2	AJ19
D14	D1	C6	AN10	AL18
D14	D1	B2	AJ16	AK15

Table 7-2. Ball Groupings/Functions

D14	D1	B3	AN13	AM19
D14	D1	B4	AK13	AN19
D14	D1	B6	AM13	AM18
D14	D1	A3	AE13	AJ15
D14	D1	A4	AL13	AN18
D14	D1	A5	AG13	AG15
D14	D1	AG4	AJ13	AE14
D14	D1	AG5	AF13	AF15
D14	D1	AG6	AH13	AH15
D14	D1	G16	L28	T28
D14	D1	G17	L29	T27
D14	D1	F15	L26	T26
D14	D1	G15	L27	T29
D14	D1	G14	L24	T23
D14	D1	F17	L25	T24
D14	D1	E15	P30	U30
D14	D1	F14	L23	T30
D14	D1	G18	P28	U28
D14	D1	E16	P29	U29
D14	D1	E18	P26	N24
D14	D1	F18	P27	N23
D14	D1	E13	P24	N25
D14	D1	G13	P25	U27
D14	D1	D17	R30	N27
D14	D1	D13	P23	U24
D14	D1	E19	R29	N26
D14	D1	G19	AJ27	AD30
D14	D1	E12	R27	U26
D14	D1	D19	R28	AD29
D14	D1	G12	R26	W30
D14	D1	F12	V29	W28
D14	D1	F11	R24	U23
D14	D1	G11	V30	W27
D14	D1	G20	R25	U25
D14	D1	D11	R23	W29
D14	D1	D20	V27	W23
D14	D1	F20	AK30	W24
D14	D1	E10	V26	W25
D14	D1	C20	V28	W26
D14	D1	F21	V23	Y30

Table 7-2. Ball Groupings/Functions

D14	D1	D10	V24	AC23
D14	D1	C17	AA29	AC24
D14	D1	G22	AA30	Y29
D14	D1	C15	AA27	Y27
D14	D1	C18	AA28	Y28
D14	D1	C14	AA25	Y26
D14	D1	G21	AA26	AC25
D14	D1	C12	AA23	Y25
D14	D1	B19	AA24	Y23
D14	D1	B9	AB29	Y24
D14	D1	C11	AB30	AC26
D14	D1	F9	AB27	AC27
D14	D1	E9	AB28	AD27
D14	D1	E21	AB26	AD28
D14	D1	G9	AB25	AD25
D14	D1	B21	AK29	AH29
D14	D1	C21	AJ29	AG29
D14	D1	B16	AK28	AH28
D14	D1	B18	AJ28	AG28
D14	D1	B12	AM28	AM29
D14	D1	B15	AL28	AL29
D14	D1	A19	AB23	AD26
D14	D1	B10	AB24	AC28
D14	D1	A16	AE29	AD24
D14	D1	A17	AE30	AC30
D14	D1	A11	AE27	AD23
D14	D1	A14	AE28	AG30
D14	D1	A8	AE25	AH30
D14	D1	A10	AE26	AC29
D14	D1	D22	AL27	AL30
D14	D1	E22	AL27	AL30
D14	D1	A22	AM27	AM8
D14	D1	B22	AM27	AM30

The test chip's 0Ω measurements, listed in Table 7-3, can be used to generate tests that can detect 0 resistance between the two points, thus adding more open test coverage.

Table 7-3. 0Ω Measurements

Shorted Ball		Shorted Ball
J1		D25
AA1		D26
AN4		AM4
AN3		AN8
F29		D28

The test chip has **VID_0-VID_5** signals pulled to VCCP with 1k resistors. Socket electrical connections can be tested by measuring resistors between the respective electrical connections. The following table can be used to generate tests that can detect 1k resistance between the two points, thus adding more open test coverage. *Rval* from Table 7-4 identifies the resistor tolerance.

Table 7-4. 1kΩ Measurements

VID Ball		Power Ball
AM2		AJ8
AL5		AG9
AM3		AH8
AL6		AF8
AK4		AF9
AL4		AG8

Each pull-down resistor can be used to verify connectivity of a ground ball and a control signal ball. The following table can be used to generate tests that can detect 1k resistance between the two points, thus adding more open test coverage. *RvalControl* from identifies the resistor tolerance.

Table 7-5. 1kΩ Measurements

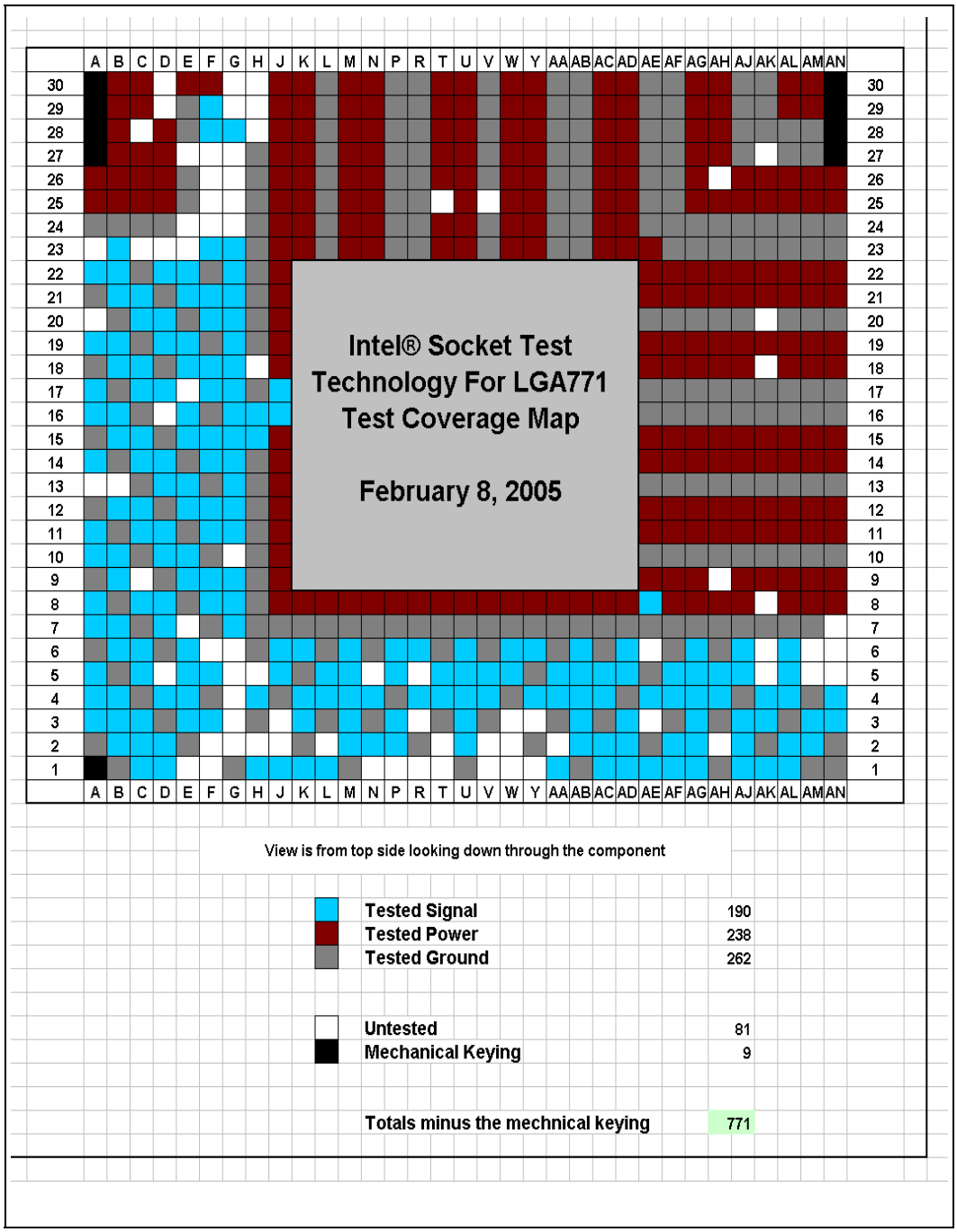
Control Resistor Ball		GND Ball
E5		U1
D1		T3
E6		E8
D14		F7

The following table can be used to generate tests that can detect 1k resistance between the two points which will add more open test coverage. *Rval* from Table 6-1 identifies the resistor tolerance.

Table 7-6. 1kΩ Measurements

Resistor Ball		Resistor Ball
J16		H13
H15		H14
H16		H17
AJ1		AJ2
AD2		AF2
AG2		AG3
AJ3		AK3
AD1		AC1
AF1		AB2
AE1		AG1
F28		G28
F3		G23
B23		C22
AL1		AK1
H1		AL2
AC2		AE8
N4		P5
AC4		AE4
AH4		AH5
AJ5		AJ6
AB3		AD3
H4		M2

Figure 7-1. Optimized Ball Coverage Map



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