Product Brief

Intel® 82574L and 82574IT Gigabit Ethernet Controllers

Network Connectivity

Intel® 82574L and 82574IT Gigabit Ethernet Controllers

Low-Power, Small-Footprint, Single-Port Gigabit Network Connectivity with Advanced Performance Features

- High-performance, low-cost, PCI Express* 10/100/1000 Ethernet Connection
- Compact 9mm x 9mm QFN Package for small-footprint embedded designs
- Fast Ethernet or Gigabit Ethernet network connectivity for single-core and multi-core CPU designs
- Low power: <710mW in GbE mode and <300mW in 10/100 mode
- Support for hardware-based time stamping of IEEE 1588 and 802.1as packets enabling high-precision time synchronization over Ethernet
- Supports 9018 Byte Jumbo Frames
- Available in Industrial Temperature: -40˚-85˚ C
- Extended lifecycle support protects system investment by providing 7-year manufacturing availability for customers
- Ideal for Embedded applications in Tele-communications Infrastructure, Industrial, Medical, Military, Interactive Client, Infotain-ment, and Print Imaging

Simple 10/100/1000 PCI-Express* (PCIe) x1 Connectivity

The Intel® 82574L/IT Gigabit Ethernet Controllers provide a pathway from legacy PCI/PCIx designs to higher performing PCIe-based designs. These single-port Controllers use a PCIe one lane (x1) interface operating at 2.5 GHz. The Intel 82574L/IT Gigabit Ethernet Controllers provide fully integrated Gigabit Ethernet Media Access Control (MAC) and Physical-Layer (PHY) capabilities that can be configured for either 1000 Mb/s or 10/100 Mb/s modes of operation. Some optional PCIe extensions are also supported in the Controllers to enhance platform capabilities for specific usage modes. Each Controller provides MDI (Copper) standard IEEE 802.3 Ethernet interface for 1000BASE-T, 100BASE-TX, and 10BASE-T applications (802.3, 802.3u, and 802.3ab). The Intel 82574L/IT also enables a quick migration from custom interconnects to Ethernet.

Architected for Small-Footprint, Low-Power Designs

The Intel 82574L/IT Gigabit Ethernet Controllers are ideal for GbE implementations on small form-factor Embedded designs as well as Client and Server LAN on Motherboard (LOM) configurations. This very small 9mm x 9mm, 64-pin, QFN (Quad Flatpack No-lead) silicon package provides a 40% reduction in total footprint over the previous generation. The Intel 82574L/IT Gigabit Ethernet Controllers consume less than 710mW in GbE mode and less than 300mW in 10/100 mode. The robust design also incorporates optional internal voltage regulation which can reduce the number of voltage supplies required from the platform to power core and I/O functions. Support of D0 and D3 power states is provided as well as Smart power-down at S0 no link and Sx no link. Support of PCIe power management wake up and Advanced power management (APM) wake up using special packets is provided as well as LAN disable function.

Filled with Performance Optimization Capabilities

The Intel 82574L/IT Gigabit Ethernet Controllers contain two transmit and two receive queues for the single port. The controller efficiently manages packets with minimum latency by combining parallel and pipelined logic architectures optimized for these independent transmit and receive queues. These queues, combined with Receive Side Scaling (RSS) and Message Signal Interrupt Extension (MSI-X) support, provide a toolset for optimizing the performance on multi-core CPU designs. Advanced interrupt-handling features to manage multiple interrupts simultaneously, combined with intelligent filtering, ordering and directing of packets to specific queues and cores, enables load-balancing the network traffic flows to improve throughput in multi-core platforms. Other performance-enhancing features include IPv4 and IPv6 checksum offload, TCP/UDP checksum offload, extended Tx descriptors for more offload capabilities, up to 256 KB TCP segmentation (TSO v2), header splitting, 40 KB packet buffer size, and 9018 Byte Jumbo Frame support.

Containing On-Board Side-Band Interfaces for Manageability

The Intel 82574L/IT Gigabit Ethernet Controllers contain an SMBus and DMTF-defined Network Controller Sideband Interface (NC-SI) for manageability. Ethernet traffic is forwarded from the network to the baseboard management controller (BMC) and vice versa using the selected sideband interface implementation. SMBus provides a legacy low-speed (100 KHz-400 KHz) serial bus to pass network traffic and also enables the BMC to configure the Controller's filters and management-related capabilities. NC-SI is an Ethernet manageability protocol which is easy to implement and offers a very fast data rate (100 Mb/s, full-duplex) interface suitable for all types of management traffic.

Packaged in an Environmentally Friendly Design

The Intel 82574L/IT Gigabit Ethernet Controllers are completely lead-free and halogen-free in their silicon and package design to reduce the potential for environmental impact.

Features	Benefits
PCI Express* Features	
PCIe* x1 interface	▪ High-bandwidth density per pin ▪ Less-congested board routing
PCIe v.1.1 (2.5 GT/s)	▪ PCI-SIG conformance and standards interoperability ▪ Supports GbE at wire speed
PCIe* advanced extensions	▪ Extended error reporting and serial number for desired usage modes
Low Power	
<750mW S0-Typ (state) 1000Base-T Active 90° C (mode) and <300mW S0-Typ (state) 100Base-T Active (mode)	▪ Low power consumption
Smart power down at S0 no link/Sx no link	▪ Power management
LAN disable function	▪ Power management
Full wake-up support: APM (formerly Wake on LAN), ACPI, and Magic Packet* wake-up enable with unique MAC address	▪ Power management
ACPI register set and power down functionality supporting D0 and D3 states	▪ Power management

Features	Benefits
Gigabit MAC/PHY Performance Features	
Integrated PHY for 10/100/1000 Mb/s for multi-speed, full, and half-duplex operation	▪ Smaller footprint and lower power dissipation compared to multiple discreet MAC and PHY solutions
Two optimized transmit (Tx) and receive (Rx) queues for the Controller's single port	▪ Efficient packet prioritization ▪ Network packet handling without waiting or buffer overflow
Descriptor ring management hardware for Transmit and Receive	▪ Optimized descriptor fetch and write-back mechanisms for efficient system memory and PCIe bandwidth usage
Legacy and Message Signal Interrupt (MSI) Modes	▪ Interrupt mapping
Message Signal Interrupt Extension (MSI-X)	▪ Advanced interrupt mapping for load balancing across multiple cores ▪ More vectors per function ▪ Software-controlled aliasing when fewer vectors are allocated than requested, and ability for each vector to use independent address and data value
Receive Side Scaling (RSS) for Windows* environment and Scalable I/O for Linux* environments (IPv4, IPv6, TCP/UDP)	▪ Two receive queues to enable traffic streams to be distributed into queues and directed to specific CPU cores
64-bit address master support for systems using more than 4 GB of physical memory	▪ Efficient use of PCIe bus and system memory
Programmable host memory receive buffer per queue (256 Bytes to 16 KBytes) and cache line size (64 Bytes to 128 Bytes)	▪ Efficient use of PCIe bus and system memory
40 KB Packet buffer size; Configurable Rx and Tx data FIFO programmable in 1 KB increments	▪ FIFO size adjustable to the application
Support for transmission and reception of packets up to 9018 Bytes (Jumbo Frames)	▪ Enables higher and better throughput of data
Compliant with 1 Gb/s Ethernet IEEE 802.3, 802.3u, 802.3ab PHY specifications	▪ Robust operation over installed base of Category-5 twisted-pair cabling
IEEE 802.3x and 802.3z compliant flow control support with software-controllable Rx thresholds and Tx pause frames	▪ Local control of network congestion levels ▪ Reduce receive buffer overflows ▪ Frame loss reduced from receive overruns
Host Offloading Features	
TCP/UDP, IPv4, and IPv6 checksum offloads; Extended Tx descriptors for more offload capabilities	▪ Improved CPU utilization
TCP Segmentation/Transmit Segmentation Offloading (TSO)	▪ Improved CPU utilization
IEEE 802.1q Virtual Local Area Network (VLAN) support with VLAN tag insertion, stripping and packet filtering for up to 4096 VLAN tags	▪ Adding (for transmits) and ping (for receives) of VLAN tags ▪ Filtering packets belonging to certain VLANs
IEEE 802.1q advanced packet filtering	▪ 16 exact-matched packets (unicast or multicast) ▪ 4096-bit hash filter for multicast frames ▪ Lower processor utilization ▪ Promiscuous (unicast and multicast) transfer mode support ▪ Optional filtering of invalid frames
Header/packet data split in receive	▪ Helps the driver to focus on the relevant part of the packet without the need to parse it
Manageability Features	
DMTF Network Controller Sideband Interface (NC-SI)	▪ Supports pass-through traffic between BMC and Controller's LAN functions ▪ Supports configuration traffic between the BMC and the Controller's internal units ▪ Allows fast data rate (up to 100 Mb/s full duplex) ▪ Allows for advanced BMC capabilities such as video redirection
SMBus pass through	▪ Enables system-level component connections for manageability purposes ▪ Enables BMC to configure the Controller's filters and management-related capabilities ▪ Data rates up to 400 KHz
Preboot eXecution Environment (PXE) flash interface support	▪ Enables system boot up via the EFI (32-bit and 64-bit) ▪ Flash interface for PXE 2.1 option ROM
iSCSI boot	▪ Enables system boot up via iSCSI ▪ Provides additional network management capability
Management Data Input/Output (MDIO) – internal management interface	▪ Enables the MAC and software to monitor and control the state of the PHY
MAC/PHY Control and Status	▪ Enhanced control capabilities through PHY reset, PHY link status, PHY duplex indication, and MAC Dx power state indication
Watchdog timer	▪ Defined by the FLASHT register to minimize Flash updates

Features / Benefits

Additional Device Features	
IEEE 1588 protocol and 802.1as implementation	▪ Time-stamping enabling precision synchronization of time-sensitive applications ▪ Distributes common time to networked media and industrial automation devices
Three output drivers on the single port to drive external LED circuits	▪ Allows event, state, or activity indication for the port ▪ Configurable for output polarity as well as blinking indicator

Characteristics	
Electrical	
Typical targeted power dissipation	▪ 702mW at 1000Base-T active ▪ 296mW at 100Base-T active
Environmental	
Operating Temperature	▪ 0° C to 85° C (82574L) ▪ -40° C to 85° C (82574IT)
Storage Temperature	▪ -40° C to 125° C
Physical	
Implemented in 90nm LP (low power) complementary metal-oxide semiconductor (CMOS) process	▪ Minimizes power and size while maintaining quality and reliability
Package	▪ 9mm x 9mm silicon package typically provides better thermal characteristics and electrical performance

Network Operating Systems (NOS) Software Support

Windows* 2000
Windows Server* 2003
Windows Server* 2008
Windows XP* (Service Pack 2) [Service Pack 3 available post-production]
Windows Vista*
RHEL* 4.6
RHEL* 5.1
Linux* Kernel version 2.6.24 or higher
Linux* Kernel version 2.4.36.2 or higher
SLES* 9 SP4
SLES* 10 SP1
DOS-NDIS2*
FreeBSD* 7.0
SCO OpenServer 6/Unixware* 7.1.x
Novell Netware* 6.5
Windows* CE (sample driver)
Windows XP Embedded (sample driver available post-production)
KITL (sample driver available post-production)
Supports PXE and iSCSI Boot

Order Codes

WG82574L	T&R: MM – 898552 Tray: MM – 898553	0–85° C Commercial Temperature
WG82574IT	T&R: MM – 898555 Tray: MM – 898556	-40–85° C Industrial Temperature

To see the full line of Intel Ethernet Controllers, visit http://www.intel.com/go/ethernet.

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