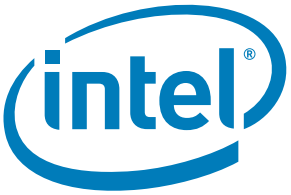

Intel® 82541ER GbE Controller Design Guide

December 2009

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Revision 2.0

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Revision History

Date	Revision	Description
December 2009	2.0	Initial public release.

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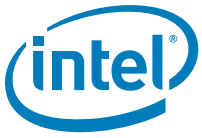

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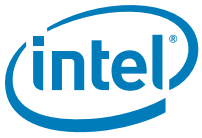


1.0 Introduction

The 82541ER Gigabit Ethernet (GbE) Controller is manufactured using a 15 mm x 15 mm, 196-ball grid array package.

1.1 Scope

This guide assumes that designers are acquainted with high-speed design and board layout techniques.

1.2 Reference Documents

The following documents provide additional information:

- 82541ER Datasheet, Intel Corporation.
- 82541GI(EI)/82547GI(EI)/82541ER EEPROM Map and Programming Information, Intel Corporation
- PCI Local Bus Specification, PCI Special Interest Group
- PCI Bus Power Management Interface Specification, Rev. 1.1, PCI Special Interest Group
- IEEE Standard 802.3, 1996 Edition, Institute of Electrical and Electronics Engineers
- IEEE Standard 802.3u, 1995 Edition, Institute of Electrical and Electronics Engineers
- IEEE Standard 802.3x, 1997 Edition, Institute of Electrical and Electronics Engineers
- IEEE Standard 802.3z, 1998 Edition, Institute of Electrical and Electronics Engineers
- IEEE Standard 802.3ab, 1999 Edition, Institute of Electrical and Electronics Engineers
- Oscillation Circuit Design Guide Application Note, Epson Electronics America, Inc. (www.eea.epson.com).
- Quartz Crystal Theory of Operation and Design Notes. Fox Electronics (www.foxonline.com).
- Crystal Technical Glossary. Fox Electronics.
- Crystal Frequently Asked Questions. Fox Electronics.
- Resonator Terminology and Formulas. Piezo Technology, Inc. (www.piezotech.com).

1.3 Product Codes

Table 1 lists the product ordering code for the 82541ER.

Table 1. Product Ordering Code

Device	Product Code	Product Code (Lead Free)
82541ER	GD82541ER	LU82541ER

2.0 Frequency Control Device Design Considerations

This section provides information regarding frequency control devices, including crystals and oscillators, for use with all Intel® Ethernet controllers. Several suitable frequency control devices are available; none of which present any unusual challenges in selection. The concepts documented herein are applicable to other data communication circuits, including Physical Layer devices (PHYs).

The Intel® Ethernet controllers contain amplifiers which, when used with the specific external components, form the basis for feedback oscillators. These oscillator circuits, which are both economical and reliable, are described in more detail in Section 4.0.

The Intel® Ethernet controllers also have bus clock input functionality, however a discussion of this feature is beyond the scope of this document, and will not be addressed.

The chosen frequency control device vendor should be consulted early in the design cycle. Crystal and oscillator manufacturers familiar with networking equipment clock requirements may provide assistance in selecting an optimum, low-cost solution.

2.1 Frequency Control Component Types

Several types of third-party frequency reference components are currently marketed. A discussion of each follows, listed in preferred order.

2.2 Quartz Crystal

Quartz crystals are generally considered to be the mainstay of frequency control components due to their low cost and ease of implementation. They are available from numerous vendors in many package types and with various specification options.

2.3 Fixed Crystal Oscillator

A packaged fixed crystal oscillator is comprised of an inverter, a quartz crystal, and passive components conveniently packaged together. The device renders a strong, consistent square wave output. Oscillators used with microprocessors are supplied in many configurations and tolerances.

Crystal oscillators should be restricted to use in special situations, such as shared clocking among devices or multiple controllers. As clock routing can be difficult to accomplish, it is preferable to provide a separate crystal for each device.

For Intel® Ethernet controllers, it is acceptable to overdrive the internal inverter by connecting a 25 MHz external oscillator to the X1 lead, leaving the X2 lead unconnected. The oscillator should be specified to drive CMOS logic levels, and the clock trace to the controller should be as short as possible. Controller specifications typically call for a 40% (minimum) to 60% (maximum) duty cycle and a ±50 ppm frequency tolerance.

2.4 Programmable Crystal Oscillators

A programmable oscillator can be configured to operate at many frequencies. The device contains a crystal frequency reference and a phase lock loop (PLL) clock generator. The frequency multipliers and divisors are controlled by programmable fuses.

A programmable oscillator's accuracy depends heavily on the Ethernet controller's differential transmit lines. The Physical Layer (PHY) uses the clock input from the device to drive a differential Manchester (for 10 Mbps operation), an MLT-3 (for 100 Mbps operation) or a PAM-5 (for 1000 Mbps operation) encoded analog signal across the twisted pair cable. These signals are referred to as self-clocking, which means the clock must be recovered at the receiving link partner. Clock recovery is performed with another PLL that locks onto the signal at the other end.

PLLs are prone to exhibit frequency jitter. The transmitted signal can also have considerable jitter even with the programmable oscillator working within its specified frequency tolerance. PLLs must be designed carefully to lock onto signals over a reasonable frequency range. If the transmitted signal has high jitter and the receiver's PLL loses its lock, then bit errors or link loss can occur.

PHY devices are deployed for many different communication applications. Some PHYs contain PLLs with marginal lock range and cannot tolerate the jitter inherent in data transmission clocked with a programmable oscillator. The American National Standards Institute (ANSI) X3.263-1995 standard test method for transmit jitter is not stringent enough to predict PLL-to-PLL lock failures, therefore, the use of programmable oscillators is generally not recommended.

3.0 Ceramic Resonator

Similar to a quartz crystal, a ceramic resonator is a piezoelectric device. A ceramic resonator typically carries a frequency tolerance of ±0.5%, – inadequate for use with Intel® Ethernet controllers, and therefore, should not be utilized.

4.0 Crystal Selection Parameters

All crystals used with Intel® Ethernet controllers are described as “AT-cut,” which refers to the angle at which the unit is sliced with respect to the long axis of the quartz stone.

Table 2 lists the crystal electrical parameters and provides suggested values for typical designs. These parameters are described in the following subsections.

Table 2. Crystal Parameters

Parameter	Suggested Value
Vibrational Mode	Fundamental
Nominal Frequency	25.000 MHz at 25° C (required)
Frequency Tolerance	±30 ppm recommended ±50 ppm across the entire operating temperature range (required by IEEE specifications)
Temperature Stability	±50 ppm at 0° C to 70° C
Calibration Mode	Parallel
Crystal Load Capacitance	16 pF to 20 pF
Shunt Capacitance	6 pF maximum
Equivalent Series Resistance	50 Ω maximum
Drive Level	0.5 mW maximum
Aging	±5 ppm per year maximum

Table 3 lists the approved crystals for use with the 82541ER C0 stepping.

Table 3. 82541ER Recommended Crystals

Manufacturer	Manufacturer's Part Number
Raltron (<20 Ω ESR and +/-30 ppm)	AS-25.000-20-F-SMD-TR
Citizen	HCM family that meets the crystal specifications.
TXC	6C25000131

4.1 Vibrational Mode

Crystals in the above-referenced frequency range are available in both fundamental and third overtone. Unless there is a special need for third overtone, use fundamental mode crystals.

At any given operating frequency, third overtone crystals are thicker and more rugged than fundamental mode crystals. Third overtone crystals are more suitable for use in military or harsh industrial environments. Third overtone crystals require a trap circuit (extra capacitor and inductor) in the load circuitry to suppress fundamental mode oscillation as the circuit powers up. Selecting values for these components is beyond the scope of this document.

4.2 Nominal Frequency

Intel® Ethernet controllers use a crystal frequency of 25.000 MHz. The 25 MHz input is used to generate a 125 MHz transmit clock for 100BASE-TX and 1000BASE-TX operation – 10 MHz and 20 MHz transmit clocks, for 10BASE-T operation.

4.3 Frequency Tolerance

The frequency tolerance for an Ethernet physical layer device is dictated by the IEEE 802.3 specification as ±50 parts per million (ppm). This measurement is referenced to a standard temperature of 25° C. Intel recommends a frequency tolerance of ±30 ppm.

4.4 Temperature Stability and Environmental Requirements

Temperature stability is a standard measure of how the oscillation frequency varies over the full operational temperature range (and beyond). Several optional temperature ranges are currently available, including -40° C to +85° C for industrial environments. Some vendors separate operating temperatures from temperature stability. Manufacturers may also list temperature stability as 50 ppm in their data sheets.

Note: Crystals also carry other specifications for storage temperature, shock resistance, and reflow solder conditions. Crystal vendors should be consulted early in the design cycle to discuss the application and its environmental requirements.

4.5 Calibration Mode

The terms “series-resonant” and “parallel-resonant” are often used to describe crystal oscillator circuits. Specifying parallel mode is critical to determining how the crystal frequency is calibrated at the factory.

A crystal specified and tested as series resonant oscillates without problem in a parallel-resonant circuit, but the frequency is higher than nominal by several hundred parts per million. The purpose of adding load capacitors to a crystal oscillator circuit is to establish resonance at a frequency higher than the crystal’s inherent series resonant frequency.

Figure 1 illustrates a simplified schematic of the 82541ER’s oscillator circuit. The crystal and the capacitors form a feedback element for the internal inverting amplifier. This combination is called parallel-resonant, because it has positive reactance at the selected frequency. In other words, the crystal behaves like an inductor in a parallel LC circuit. Oscillators with piezoelectric feedback elements are also known as “Pierce” oscillators.

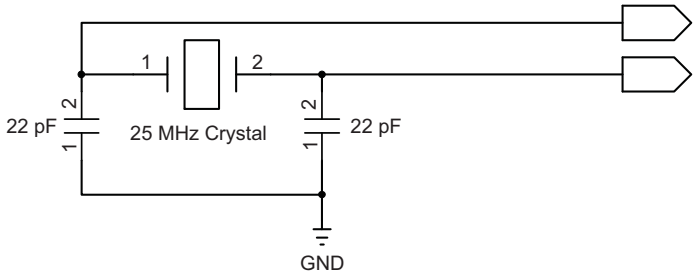


Figure 1. 82541ER Oscillator Circuit

4.6 Load Capacitance

The formula for crystal load capacitance is as follows:

$$C_L = \frac{(C1 \cdot C2)}{(C1 + C2)} + C_{stray}$$

where C1 = C2 = 22 pF (as suggested in most Intel reference designs)

and C_{stray} = allowance for additional capacitance in pads, traces and the chip carrier within the Ethernet controller package

An allowance of 3 pF to 7 pF accounts for lumped stray capacitance. The calculated load capacitance is 16 pF with an estimated stray capacitance of about 5 pF.

Individual stray capacitance components can be estimated and added. For example, surface mount pads for the load capacitors add approximately 2.5 pF in parallel to each capacitor. This technique is especially useful if Y1, C1 and C2 must be placed farther than approximately one-half (0.5) inch from the controller. It is worth noting that thin circuit boards generally have higher stray capacitance than thick circuit boards.

Standard capacitor loads used by crystal manufacturers include 16 pF, 18 pF and 20 pF. Any of these values will generally operate with the controller. However, a difference of several picofarads between the calibrated load and the actual load will pull the oscillator slightly off frequency.

The oscillator frequency should be measured with a precision frequency counter where possible. The load specification or values of C1 and C2 should be fine tuned for the design. As the actual capacitance load increases, the oscillator frequency decreases.

Note: C1 and C2 may vary by as much as 5% from their nominal values.

4.7 Shunt Capacitance

The shunt capacitance parameter is relatively unimportant compared to load capacitance. Shunt capacitance represents the effect of the crystal's mechanical holder and contacts. The shunt capacitance should equal a maximum of 6 pF (7 pF is also acceptable).

4.8 Equivalent Series Resistance

Equivalent Series Resistance (ESR) is the real component of the crystal's impedance at the calibration frequency, which the inverting amplifier's loop gain must overcome. ESR varies inversely with frequency for a given crystal family. The lower the ESR, the faster the crystal starts up. Use crystals with an ESR value of 50 Ω or better.

Note: Check the specific controller documentation carefully; some devices may have tighter ESR requirements.

4.9 Drive Level

Drive level refers to power dissipation in use. The allowable drive level for a Surface Mounted Technology (SMT) crystal is less than its through-hole counterpart, because surface mount crystals are typically made from narrow, rectangular AT strips, rather than circular AT quartz blanks.

Some crystal data sheets list crystals with a maximum drive level of 1 mW. However, Intel® Ethernet controllers drive crystals to a level less than the suggested 0.5 mW value. This parameter does not have much value for on-chip oscillator use.

4.10 Aging

Aging is a permanent change in frequency (and resistance) occurring over time. This parameter is most important in its first year because new crystals age faster than old crystals. Use crystals with a maximum of ±5 ppm per year aging.

4.11 Reference Crystal

The normal tolerances of the discrete crystal components can contribute to small frequency offsets with respect to the target center frequency. To minimize the risk of tolerance-caused frequency offsets causing a small percentage of production line units to be outside of the acceptable frequency range, it is important to account for those shifts while empirically determining the proper values for the discrete loading capacitors, C1 and C2.

Even with a perfect support circuit, most crystals will oscillate slightly higher or slightly lower than the exact center of the target frequency. Therefore, frequency measurements (which determine the correct value for C1 and C2) should be performed with an ideal reference crystal. When the capacitive load is exactly equal to the crystal's load rating, an ideal reference crystal will be perfectly centered at the desired target frequency.

4.12 Reference Crystal Selection

There are several methods available for choosing the appropriate reference crystal:

- If a Saunders and Associates (S&A) crystal network analyzer is available, then discrete crystal components can be tested until one is found with zero or nearly zero ppm deviation (with the appropriate capacitive load). A crystal with zero or near zero ppm deviation will be a good reference crystal to use in subsequent frequency tests to determine the best values for C1 and C2.
- If a crystal analyzer is not available, then the selection of a reference crystal can be done by measuring a statistically valid sample population of crystals, which has units from multiple lots and approved vendors. The crystal, which has an oscillation frequency closest to the center of the distribution, should be the reference crystal used during testing to determine the best values for C1 and C2.
- It may also be possible to ask the approved crystal vendors or manufacturers to provide a reference crystal with zero or nearly zero deviation from the specified frequency when it has the specified CLoad capacitance.

When choosing a crystal, customers must keep in mind that to comply with IEEE specifications for 10/100/1000Base-T Ethernet LAN, the transmitter reference frequency must be precise within ±50 ppm. Intel® recommends customers to use a transmitter reference frequency that is accurate to within ±30 ppm to account for variations in crystal accuracy due to crystal manufacturing tolerance. For information about measuring transmitter reference frequency, refer to Appendix A.

4.12.1 Circuit Board

Since the dielectric layers of the circuit board are allowed some reasonable variation in thickness, the stray capacitance from the printed board (to the crystal circuit) will also vary. If the thickness tolerance for the outer layers of dielectric are controlled within ±17 percent of nominal, then the circuit board should not cause more than ±2 pF variation to the stray capacitance at the crystal. When tuning crystal frequency, it is recommended that at least three circuit boards are tested for frequency. These boards should be from different production lots of bare circuit boards.

Alternatively, a larger sample population of circuit boards can be used. A larger population will increase the probability of obtaining the full range of possible variations in dielectric thickness and the full range of variation in stray capacitance.

Next, the exact same crystal and discrete load capacitors (C1 and C2) must be soldered onto each board, and the LAN reference frequency should be measured on each circuit board.

The circuit board, which has a LAN reference frequency closest to the center of the frequency distribution, should be used while performing the frequency measurements to select the appropriate value for C1 and C2.

4.12.2 Temperature Changes

Temperature changes can cause the crystal frequency to shift. Therefore, frequency measurements should be done in the final system chassis across the system's rated operating temperature range.

5.0 Ethernet Component Design Guidelines

This section provides recommendations for selecting components and connecting special pins. The main design elements are the 82541ER Gigabit Ethernet Controller, a magnetics module with RJ-45 connector, and a crystal clock source.

5.1 Designing with the 82541ER Gigabit Controllers

This section provides design guidelines specific to the 82541ER Gigabit Ethernet Controllers.

5.1.1 82541ER Ethernet Controller LAN Disable Guidelines

The 82541ER controller has a LAN disable function that is present on FLSH_SO, ball P9. This pin can be connected to a General Purpose I/O (GPIO) pin to enable the BIOS to disable the Ethernet port. If the serial Flash interface is populated, the Flash serial output pin must not interfere with this function.

Do not attempt to use the LAN_POWER_GOOD signal for a LAN disable input on the 82541ER device. This pin is intended to operate as a power-on reset connected to a power monitor circuit.

The input of the 82541ER FLSH_SO (pin P9) is the LAN_DISABLE# signal. It is sampled on the rising edge of LAN_PWR_GOOD or RST#. The signal must be held valid for 80 ns after either rising edge.

If it is sampled high, the LAN functions normally. If it is sampled low, then the following occurs:

1. The LAN is disabled.
2. The PHY is powered down.
3. Most MAC clock domains are gated.
4. Most functional blocks are held in reset.
5. PCI inputs and outputs are floated.
6. The device will not respond to PCI cycles (including configuration cycles).
7. The device is put in a low power state, which is equivalent to D3 without wakeup or manageability.

5.1.2 Power Supplies for the 82541ER Controller

The 82541ER controller requires three power supplies: 1.2 V, 1.8 V, and 3.3 V. The 1.2 V supply must provide approximately 500 mA current, and the 1.8 V supply, approximately 230 mA current. The 3.3 V supply must provide only 30 mA current.

A central power supply can provide all the required voltage sources, or the power can be derived and regulated locally near the Ethernet control circuitry. All voltage sources must remain present during lower power states in order to use the 82541ER LAN wake up capability. This consideration makes it more likely that at least some of the voltage sources will be local.

Instead of using external regulators to supply 1.2 V and 1.8 V, power transistors can be used in conjunction with on-chip regulation circuitry. (See the reference schematic for an implementation example.)

The 82541ER controller has a LAN_PWR_GOOD input. Treat this signal as an external device reset which works in conjunction with the internal power-on reset circuitry. In the situation where a central power supply furnishes all the voltage sources, LAN_PWR_GOOD can be tied to the POWER_GOOD output of the power supply. Designs that generate some of the voltages locally can connect LAN_PWR_GOOD to a power monitor chip.

5.1.3 Power Sequencing

The power sources are all expected to ramp up during a brief power-up interval (approximately 20 ms) with LAN_PWR_GOOD de-asserted. The 82541ER controller must not be left in a prolonged state where some, but not all, voltages are applied. Note that:

- The 3.3 V source should be powered up prior to the 1.2 V or 1.8 V sources.
- The 1.2 V and 1.8 V power supplies may power up simultaneously.
- At any time during power up, the supply voltages must be: 1.2 V < 1.8 V < 3.3 V.

5.1.4 82541ER Controller Power Supply Filtering

The 82541ER controller switches relatively high currents at high frequencies, requiring generous use of both bulk capacitance and high speed decoupling capacitance adjacent to the device.

Bypass capacitors for each power rail should be 0.1 µF. If possible, orient the capacitors close to the device and adjacent to power pads. Decoupling capacitors should connect to the power and ground planes with short, thick traces (15 mils or 0.4 mm or more), and 14 mil (3.5 mm) vias per capacitor pad.

Furnish approximately 20 µF of bulk capacitance for each of the main 1.2 V and 1.8 V levels. This can be easily achieved by using two 10 µF capacitors, placing them as close to the device power connections as possible.

5.1.5 82541ER Controller Power Management and Wake Up

The 82541ER Gigabit Ethernet Controller supports low power operation as defined in the PCI Bus Power Management Specification. There are two defined power states, D0 and D3. The D0 state provides full power operation and is divided into two sub-states: D0u (uninitialized) and D0a (active). The D3 state provides low power operation and is also divided into two sub-states: D3hot and D3cold.

To enter the low power state, the software driver must stop data transmission and reception. Either the operating system or the driver must program the Power Management Control/Status Register (PMCSR) and the Wakeup Control Register (WUC). If wakeup is desired, the appropriate wakeup LAN address filters must also be set. The initial power management settings are specified by EEPROM bits.

When the 82541ER controller transitions to either of the D3 low power states, the 1.2 V, 1.8 V, and 3.3 V sources must continue to be supplied to the device. Otherwise, it will not be possible to use a wakeup mechanism. The AUX_POWER signal is a logic input to the 82541ER controller that denotes auxiliary power is available. If AUX_POWER is asserted, the 82541ER device will advertise that it supports wake up from a D3cold state.

The 82541ER device supports both Advanced Power Management (APM) wakeup and Advanced Configuration and Power Interface (ACPI) wakeup. APM wakeup has also been known in the past as “Wake on LAN.”

Wakeup uses the PME# signal to wake the system. PME# is an active low signal connected to a GPIO port on the ICH5 that goes active in response to receiving a Magic Packet*, a network wake-up packet, or link status change indication. PME# remains asserted until it is disabled through the Power Management Control/Status Register.

5.1.6 82541ER Device Test Capability

The 82541ER Gigabit Ethernet Controller contains a test access port conforming to the IEEE 1149.1a-1994 (JTAG) Boundary Scan specification. To use the test access port, these balls need to be connected to pads accessible by the test equipment. The TRST# input also needs to be connected to ground through a pull-down resistor (approximately 100 Ω) so that the test capability cannot be invoked by mistake.

A Boundary Scan Definition Language (BSDL) file describing the 82541ER device is available for use in your test environment. Contact your Intel representative for more details.

The controller also contains an XOR test tree mechanism for simple board tests. Details of XOR tree operation may be obtained through your Intel representative.

5.1.7 82541ER Oscillator Solution

There are two oscillator solutions for the 82541ER: high voltage and low voltage.

5.1.7.1 High Voltage Solution (VDD = 3.3 V)

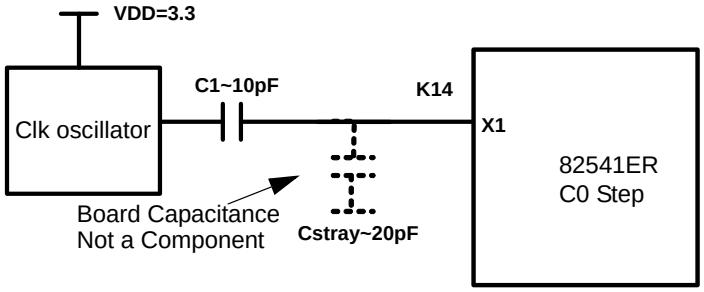
This solution involves capacitor C1, which forms a capacitor divider with C_{stray} of about 20 pF. This attenuates the input clock amplitude and adjusts the clock oscillator load capacitance.

$$V_{in} = VDD * (C1/(C1 + C_{stray}))$$
$$V_{in} = 3.3 * (C1/(C1 + C_{stray}))$$

This enables load clock oscillators of 15 pF to be used. If the value of C_{stray} is unknown, C1 should be adjusted by tuning the input clock amplitude to approximately 1 V_{ptp}. If C_{stray} equals 20 pF, then C1 is 10 pF ±10%.

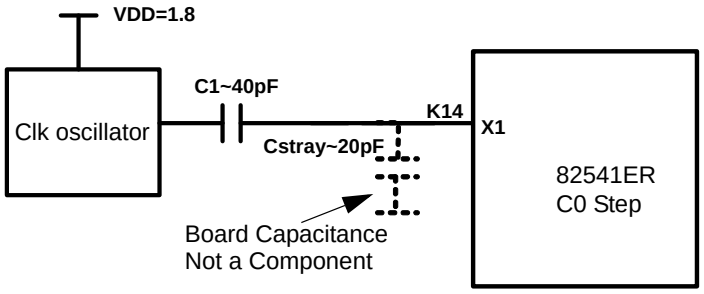
A low capacitance, high impedance probe (C < 1 pF, R > 500 K Ω) should be used for testing. Probing the parameters can affect the measurement of the clock amplitude and cause errors in the adjustment. A test should also be done after the probe has been removed for circuit operation.

If jitter performance is poor, a lower jitter clock oscillator can be implemented.



5.1.7.2 Low Voltage Solution (VDD = 1.8 V)

The low voltage solution is similar to the high voltage solution. However, the low voltage includes a low consumption and low jitter clock oscillator that uses a 1.8 V external power supply. In this case, C1 will require adjusting according to the stray capacitance from X1.



6.0 PCB Routing Guidelines

6.1 Critical Dimensions for Discrete Magnetics Module and RJ-45

There are four critical dimensions that must be considered during the layout phase of an 82541ER LAN On Motherboard (LOM) implementation. These dimensions are identified in Figure 2 as A, B, C and D.

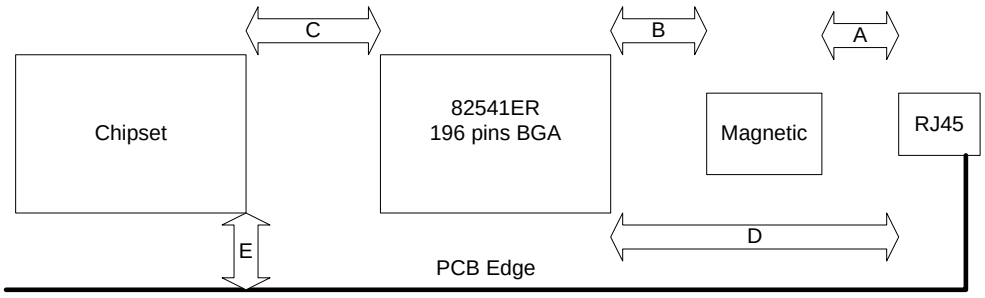


Figure 2. Critical Dimensions for 82541ER Component Placement

6.1.1 Distance A: Magnetics to RJ-45

The distance labeled “A” in Figure 1 should be given highest priority in board layout. The distance between the magnetics and RJ-45 should be less than 1 inch of separation. The following trace characteristics are important and should be observed.

- Differential Impedance: The differential impedance should be 100 Ω. The single ended trace impedance will be approximately 50 Ω; however, the differential impedance can also be affected by the spacing between the traces.
- Trace Symmetry: Differential pairs should be routed with consistent separation and with exactly the same lengths and physical dimensions.

6.1.2 Distance B: GbE Controller to Magnetics

The distance labeled “B” should also be designed to be less than one inch between devices. The high-speed nature of the signals propagating through the traces requires that the distance between these components be closely observed. In general, any section of traces intended for use with high-speed signals should observe proper termination practices. Proper termination of signals can reduce reflections caused by impedance mismatches between devices and traces.

6.1.3 Terminating Differential Pairs for 82541ER-Based Designs

Four differential pairs are terminated using 49.9 Ω (1% tolerance) resistors, placed near the GbE controller. One resistor connects to the MDI+ (MDI positive) signal trace and another resistor connects to the MDI- (MDI negative) signal trace. The opposite ends of the resistors connect together and to ground through a single 0.1 µF capacitor. The capacitor should be placed as close as possible to the 49.9 Ω resistors, using a wide trace.

Note: Do not vary the suggested component values. Be sure to lay out symmetrical pads and traces for these components such that the length and symmetry of the differential pairs are not disturbed.

6.1.4 Distance C: GbE Controller to Chipset

The PCI bus on 82541ER meets PCI 2.3 specification. The trace routing on the bus should follow the appropriate PCI specification.

The Ethernet controllers operate as PCI slave devices for configuration and register programming. After the devices have been properly initialized, they can also operate as PCI masters to fetch memory descriptors and to read/write data buffers.

The devices are capable of operating in either a 5 V or 3.3 V signaling environment. The VIO terminals can be connected to either 3.3 V or 5 V to choose the appropriate PCI bus levels.These connections bias the controller PCI I/O buffers for the correct switching strength. However, all other digital inputs and outputs use 3.3 V signaling unless specified separately.

6.1.5 Distance D: The Overall Length of Differential Traces from LAN to RJ-45

The overall length of differential pairs should be less than four inches measured from the GbE controller to RJ-45 through the magnetics module.

The lengths of the differential traces (within each pair) should be equal within 50 mils (1.25 mm) and as symmetrical as possible.

6.1.6 Distance E: GbE Controller to PCB Edge

The GbE controller should be placed at least two inches from the printed circuit board edge.

6.2 Critical Dimensions for an Integrated Magnetics Module

6.2.1 Distance A: The Overall Length of Differential Traces

The overall length of differential pairs should be less than four inches measured from the GbE controller across the magnetics module to the RJ-45 connector (see Figure 6.2.1).

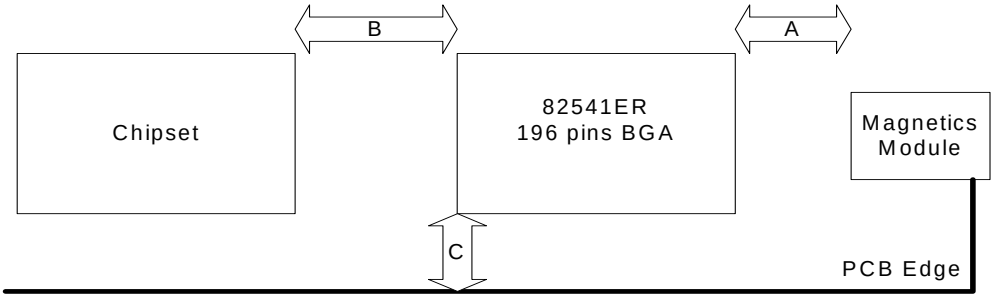


Figure 3. Critical Dimensions for 82541ER Component Placement with Integrated Magnetics Module

6.2.2 Distance B: GbE Controller to Chipset

For PCI bus on the 82541ER, the bus routing should meet the PCI 2.3 specification.

6.2.3 Distance C: GbE Controller to PCB Edge

The GbE controller should be placed at least one inch from the PCB edge.

6.3 General LAN Differential Pair Trace Routing Considerations

Trace routing considerations are important to minimize the effects of crosstalk and propagation delays on sections of the board where high-speed signals exist. Signal traces should be kept as short as possible to decrease interference from other signals, including those propagated through power and ground planes.

Observe the following suggestions to help optimize board performance (Note: Some suggestions are specific to a 4.3 mil stackup.):

- Maintain constant symmetry and spacing between the traces within a differential pair.
- Keep the signal trace lengths of a differential pair equal to each other.

- Keep the total length of each differential pair under four inches. Many customer designs with differential traces longer than five inches have had one or more of the following issues:
  - IEEE PHY conformance failures
  - Excessive Electro Magnetic Interference (EMI)
  - Degraded receive Bit Error Rate (BER)
- Do not route the transmit differential traces closer than 100 mils to the receive differential traces.
- Do not route any other signal traces both parallel to the differential traces and closer than 100 mils to the differential traces (300 mils is recommended).
- Keep maximum separation between differential pairs to seven mils.
- For high-speed signals, the number of corners and vias should be kept to a minimum. If a 90° bend is required, it is recommended to use two 45° bends instead.
- Traces should be routed away from board edges by a distance greater than the trace height above the ground plane. This allows the field around the trace to couple more easily to the ground plane rather than to adjacent wires or boards.
- Do not route traces and vias under crystals or oscillators. This prevents coupling to or from the clock. And as a general rule, place traces from clocks and drives at a minimum distance from apertures by a distance that is greater than the largest aperture dimension.

6.3.1 Trace Routing and Geometry

The key factors in controlling trace EMI radiation are the trace length and the ratio of trace-width to trace-height above the ground plane (see Figure 4). To minimize trace inductance, high-speed signals and signal layers that are close to a ground or power plane should be as short and wide as practical. Ideally, this trace width to height above the ground plane ratio is between 1:1 and 3:1. To maintain trace impedance, the width of the trace should be modified when changing from one board layer to another if the two layers are not equidistant from the power or ground plane. Differential trace impedances should be controlled to be ~100 Ω. It is necessary to compensate for trace-to-trace edge coupling, which can lower the differential impedance by up to 10 Ω, when the traces within a pair are closer than 30 mils (edge-to-edge).

Traces between decoupling and I/O filter capacitors should be as short and wide as practical. Long and thin traces are more inductive and would reduce the intended effect of decoupling capacitors. Also for similar reasons, traces to I/O signals and signal terminations should be as short as possible. Vias to the decoupling capacitors should be sufficiently large in diameter to decrease series inductance. Additionally, the GbE controller should not be closer than one inch to the connector/magnetics/edge of the board.

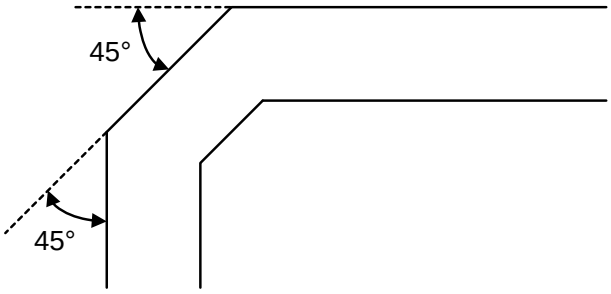


Figure 4. Trace Routing

6.3.1.1 Signal Isolation

Some rules to follow for signal isolation:

- Separate and group signals by function on separate layers if possible. Maintain a gap of 100 mils between all differential pairs (Ethernet) and other nets, but group associated differential pairs together.

Note: Over the length of the trace run, each differential pair should be at least 0.3 inches away from any parallel signal traces.

- Physically group together all components associated with one clock trace to reduce trace length and radiation.
- Isolate I/O signals from high speed signals to minimize crosstalk, which can increase EMI emission and susceptibility to EMI from other signals.
- Avoid routing high-speed LAN traces near other high-frequency signals associated with a video controller, cache controller, CPU, or other similar devices.

6.3.1.2 Magnetics Module General Power and Ground Plane Considerations

To properly implement the common mode choke functionality of the magnetics module the chassis or output ground (secondary side of transformer) should be separated from the digital or input ground (primary side) by a physical separation of 100 mils minimum.

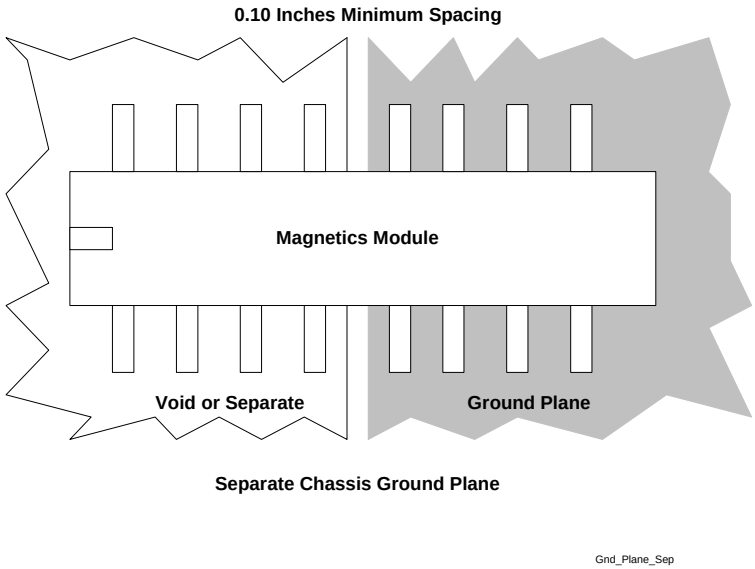


Figure 5. Separate Chassis Ground Plane

6.3.1.3 Separation

Good grounding requires minimizing inductance levels in the interconnections and keeping ground returns short, signal loop areas small, and power inputs bypassed to signal return, will significantly reduce EMI radiation.

Follow these rules to help reduce circuit inductance in both back planes and motherboards:

Route traces over a continuous plane with no interruptions (don't route over a split plane). If there are vacant areas on a ground or power plane, avoid routing signals over the vacant area. This increases inductance and EMI radiation levels.

Separate noisy digital grounds from analog grounds to reduce coupling. Noisy digital grounds can affect sensitive DC subsystems.

All ground vias should be connected to every ground plane. In addition, every power via should be connected to all power planes at equal potential. This helps reduce circuit inductance.

Physically locate grounds between a signal path and its return. This minimizes the loop area.

Avoid fast rise/fall times as much as possible. Signals with fast rise and fall times contain many high frequency harmonics which can radiate EMI.

- The ground plane beneath the filter/transformer module should be split (see Figure 5). The RJ-45 connector side of the transformer module should have chassis ground beneath it. By splitting ground planes beneath transformer, noise coupling between the primary and secondary sides of the transformer and between the adjacent coils in the transformer is minimized. There should not be a power plane under the magnetics module.

6.4 Schematic for EEPROM Footprint

Figure 6 shows the EEPROM footprint for the 82541ER.

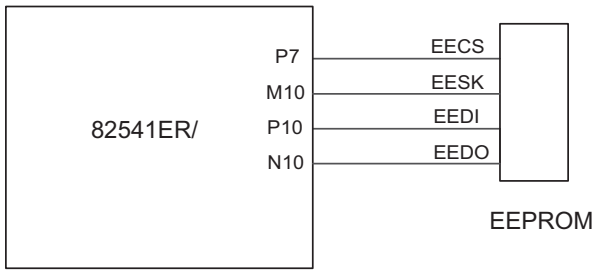


Figure 6. 82541ER EEPROM Footprint

7.0 Selecting a Magnetics Module for 10/100/1000 LOM Designs

7.1 Qualifying Magnetics for an 82541ER LOM Design

One of the most important component choices in a GbE controller LOM design is the magnetics module. The module has a critical effect on overall IEEE and emission compliance. The device selected should meet the required design performance. Occasionally, components that meet basic specifications can cause the system (LOM, NIC, Repeater, etc.) to fail because of unintentional interactions with board effects. Examples of these phenomena could be an unexpected series of parallel capacitance values or expected series inductance values within the magnetics module. This can cause the design to fail certain IEEE specifications.

In order to help OEMs qualify a magnetics module, Intel provides the electrical specifications for magnetics modules used with Intel's LOM or NIC designs as a reference (refer to Table 4 and Table 5).

Note: Table 4 lists the LAN magnetics that have been used successfully in some applications but might not be successful for all applications.

Table 4. LAN Magnetics Modules

Vendor	Magnetics Module	Integrated/Discrete	If Integrated, With or Without USB?
Pulse*	H5007	Discrete	
Bel*	S558-5999-P3	Discrete	
We-Midcom*	000-7412-35	Discrete	
Pulse	JY0-0019NL	Integrated	Yes (2)
Bel	0862-1J1T-43	Integrated	No
Bel	0826-1XLT-23	Integrated	No
Pulse	JW0A2P019D	Integrated	Yes (2)
SpeedTech*	P25-BFB4-RDW9	Integrated	Yes (2)
Tyco*	1840023-1	Integrated	Yes (2)

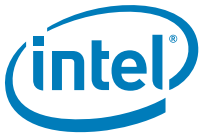


Table 5. Electrical Specifications at 25° C for GbE Silicon

Insertion Loss (TX / RX)	
0.1 through 999 kHz	1.0 dB maximum
1.0 through 60.0 MHz	0.6 dB maximum
60.1 through 80.0 MHz	0.8 dB maximum
80.1 through 100.0 MHz	1.0 dB maximum
100 through 125.0 MHz	2.4 dB maximum
Return Loss (TX / RX)	
1.0 through 40.0 MHz	18 dB minimum
40.1 through 100 MHZ	12 - [20Log(f/80 MHz)] dB minimum
Common Mode-to-Common Mode Rejection	
1.0 through 60 MHz	48 dB minimum
60.1 through 100 MHz	42 dB minimum
100.1 through 150 MHz	37 dB minimum
Differential-to-Common Mode Rejection	
1.0 through 60 MHz	35 dB minimum
60.1 through 100 MHz	29 dB minimum
100.1 through 150 MHz	22 dB minimum
Crosstalk Isolation (TX / RX)	
1.0 through 80 MHz	36 dB minimum
80.1 through 150 MHz	27dB minimum
High Voltage Isolation	
1500 Vrms minimum, at 50 to 60 Hz, for 60 sec.	2250 V dc for 60 seconds
OCL with 8 mA Bias	400 uH minimum

8.0 EEPROM Information

82541ER EEPROMs are used for hardware and software configuration and are read by software to determine specific design features.

8.1 Serial EEPROM for 82541ER Controller Implementations

82541ER Gigabit Ethernet Controllers can use either a Microwire* or an SPI* serial EEPROM. The EEPROM mode is selected on the EEMODE input (pin J4). A no connect denotes an SPI EEPROM and a 100 Ω pull-down resistor to ground denotes a Microwire EEPROM. Several words of the EEPROM are accessed automatically by the device after reset to provide pre-boot configuration data before it is accessed by host software. The remainder of the EEPROM space is available to software for storing the MAC address, serial numbers, and additional information.

For non-ASF applications, a 64 register by 16-bit Microwire serial EEPROM should be used, and for ASF 1.0 applications, a larger 93C66 Microwire or AT25040 SPI serial EEPROM. ASF 2.0 requires an 8 KB SPI serial EEPROM.

The EEPROM access algorithm programmed into the 82541ER controller is compatible with most, but not all, commercially available 3.3 V Microwire* interface, serial EEPROM devices, with 64 x 16 (or 256 x 16) organization and a 1 MHz speed rating. The 82541ER EEPROM access algorithm drives extra pulses on the shift clock at the beginnings and ends of read and write cycles. The extra pulses may violate the timing specifications of some EEPROM devices. In selecting a serial EEPROM, choose a device that specifies “don't care” shift clock states between accesses.

Microwire EEPROMs that have been found to work satisfactorily with the 82541ER Gigabit Ethernet Controller are listed in Table 6.

Table 6. Microwire 64 x 16 Serial EEPROMs

Manufacturer	Manufacturer's Part Number
Atmel	AT93C46[1]
Catalyst	CAT93C46[1,2]

1. No manageability provided.
2. Revision H is not supported. Product die revision letter is marked on top of the package as a suffix to the production data code (e.g., AYWW**H**.)

SPI EEPROMs that have been found to work satisfactorily with the 82541ER device are listed in Table 7. SPI EEPROMs must be rated for a clock rate of at least 2 MHz.

Table 7. SPI Serial EEPROMs for 82541ER Controller

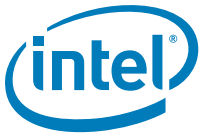
Application	Manufacturer	Manufacturer's Part Number
ASF 1.0 or IMPI pass through	ATMEL	AT25040
ASF 2.0 or IMPI advanced pass through	ATMEL	AT25080

8.1.1 EEPROM Map Information

Table 8 lists the EEPROM map for the 82541ER Gigabit Ethernet Controller. For details on the EEPROM, refer to the *Intel® 82547GI(EI)/82541(PI/GI/EI)/82541ER EEPROM Map and Programming Information*.

Table 8. 82541ER EEPROM Memory Layout

00h **3Fh**	HW/SW Reserved Area
40h **FFh**	ASF and Legacy Manageability
100h **19F**	Manageability Packet Filter Data
1A0 **...** **EEPROM END**	Loadable Manageability Firmware Code



9.0 Pin Number to Signal Mapping with Population Options

Table 9 lists the pin names for the 82541ER. Note that the pin name in the 82541ER Datasheet/Design Guide is slightly different from the signal name on the reference schematics. The Datasheet/Design Guide signal names maintain consistency with the 64-bit GbE controller naming conventions, while the schematic names follow the conventions used by our engineers on their design tools.

Table 9. 82541ER Ball Number to Signal Mapping (Sheet 1 of 2)

Ball Ref	Pin Name	Ball Ref	Pin Name	Ball Ref	Pin Name	Ball Ref	Pin Name
A1	NC	C12	AVSS	F9	VSS	J6	1.2 V
A2	SERR#	C13	MDI[0+]	F10	VSS	J7	1.2 V
A3	VCC	C14	MDI[0-]	F11	AVSS	J8	1.2 V
A4	IDSEL	D1	AD[18]	F12	NC	J9	1.2 V
A5	AD[25]	D2	AD[19]	F13	MDI[2]+	J10	1.2 V
A6	NC	D3	AD[20]	F14	MDI[2]-	J11	1.2 V
A7	VCC	D4	VSS	G1	CLK	J12	AUX_PWR
A8	AD[30]	D5	VSS	G2	VIO	J13	XTAL_1.8 V
A9	LAN_PWR_GOOD	D6	VSS	G3	TRDY#	J14	XTAL2
A10	Pull up to VCC	D7	VSS	G4	PLL_1.2 V	K1	AD[16]
A11	VCC	D8	VSS	G5	1.2 V	K2	VSS
A12	LINK_LED#	D9	NC	G6	1.2 V	K3	VCC
A13	TEST	D10	NC	G7	VSS	K4	VCC
A14	NC	D11	ANALOG_1.8 V	G8	VSS	K5	1.2 V
B1	AD[22]	D12	CLKR_1.8 V	G9	VSS	K6	1.2 V
B2	AD[23]	D13	AVSS	G10	VSS	K7	1.2 V
B3	VSS	D14	IEEE_TEST-	G11	AVSS	K8	1.2 V
B4	AD[24]	E1	VCC	G12	ANALOG_1.8 V	K9	1.2 V
B5	AD[26]	E2	VSS	G13	ANALOG_1.2 V	K10	1.2 V
B6	AD[27]	E3	AD[17]	G14	AVSS	K11	1.2 V
B7	VSS	E4	VSS	H1	STOP#	K12	AVSS
B8	AD[31]	E5	VSS	H2	INTA#	K13	VCC
B9	RST#	E6	VSS	H3	DEVSEL#	K14	XTAL1
B10	Pull up to VCC	E7	VSS	H4	PLL_1.2 V	L1	AD[14]
B11	LINK100#	E8	VSS	H5	1.2 V	L2	AD[15]
B12	LINK1000#	E9	VSS	H6	1.2V	L3	C/BE#[1]
B13	CTRL18	E10	VSS	H7	1.2V	L4	1.2 V
B14	IEEE_TEST+	E11	ANALOG_1.2V	H8	1.2V	L5	1.2 V
C1	AD[21]	E12	ANALOG_1.2V	H9	VSS	L6	VSS
C2	M66EN	E13	MDI[1]+	H10	VSS	L7	NC
C3	REQ#	E14	MDI[1]-	H11	ANALOG_1.2V	L8	NC
C4	C/BE#[3]	F1	IRDY#	H12	NC	L9	1.2 V
C5	NC	F2	FRAME#	H13	MDI[3]+	L10	1.2 V
C6	AD[28]	F3	C/BE#[2]	H14	MDI[3]-	L11	VSS
C7	AD[29]	F4	VSS	J1	PAR	L12	JTAG_TMS
C8	NC	F5	VSS	J2	PERR#	L13	JTAG_TRST#
C9	Pull up to VCC	F6	VSS	J3	GNT#	L14	JTAG_TCK
C10	VSS	F7	VSS	J4	EEMODE	M1	AD[11]
C11	ACTIVITY#	F8	VSS	J5	1.2 V	M2	AD[12]

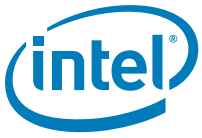


Table 9. 82541ER Ball Number to Signal Mapping (Sheet 2 of 2)

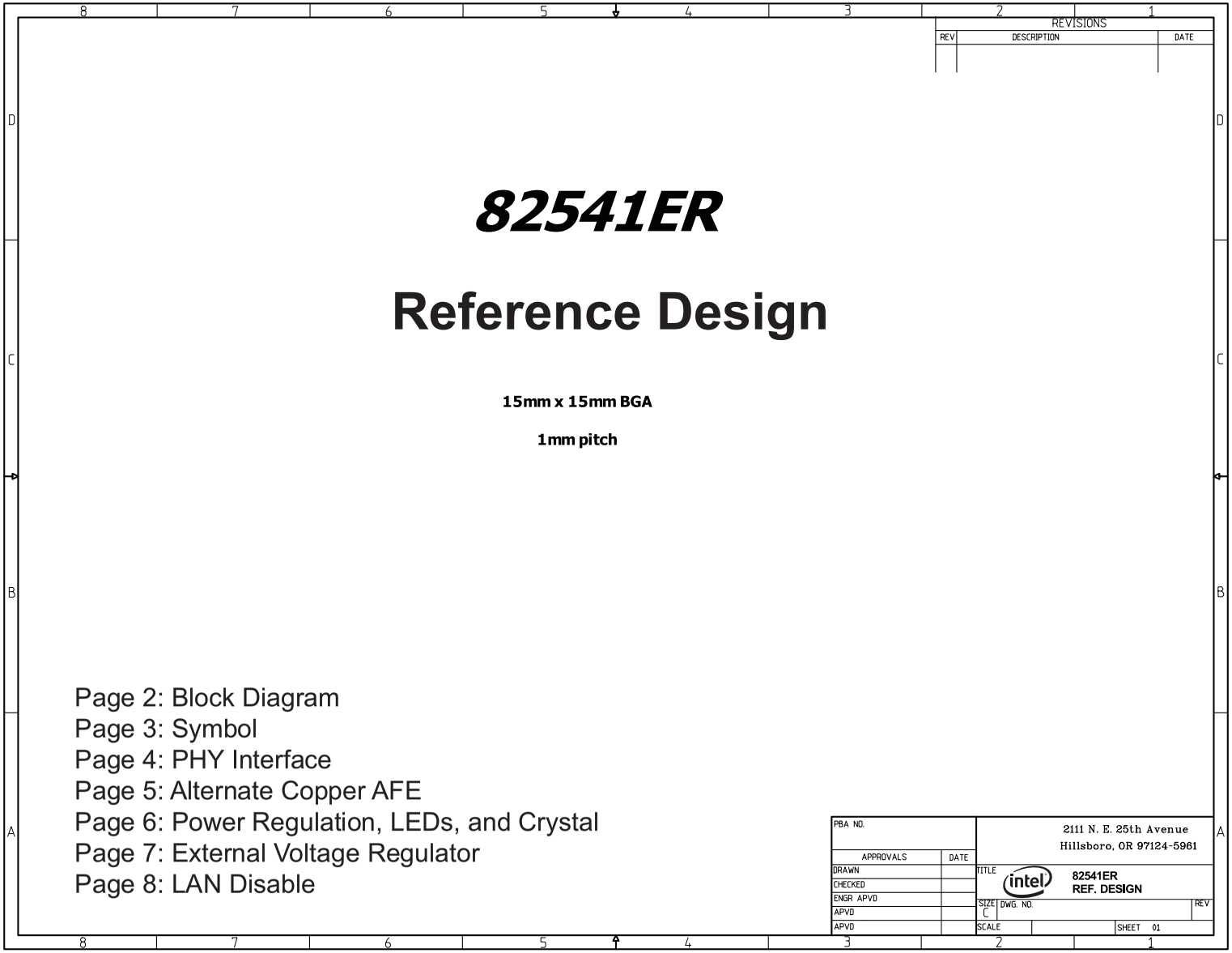
Ball Ref	Pin Name	Ball Ref	Pin Name	Ball Ref	Pin Name	Ball Ref	Pin Name
M3	AD[13]	M13	JTAG_TDI	N9	FLSH_SCK	P5	AD[3]
M4	C/BE#[0]	M14	JTAG_TDO	N10	EEDO	P6	AD[2]
M5	AD[5]	N1	VSS	N11	NC	P7	EECS
M6	VSS	N2	AD[10]	N12	VSS	P8	VSS
M7	AD[1]	N3	AD[9]	N13	SDP[2]	P9	FLSH_SO
M8	NC	N4	AD[7]	N14	SDP[0]	P10	EEDI
M9	FLSH_CE#	N5	AD[4]	P1	NC	P11	CTRL12
M10	EESK	N6	VCC	P2	VCC	P12	VCC
M11	FLSH_SI	N7	AD[0]	P3	AD[8]	P13	SDP[1]
M12	SDP[3]	N8	VCC	P4	AD[6]		

10.0 Schematic and Board Layout Checklists

A Portable Data Format (PDF) schematic and board layout checklist is available to aid designers via http://developer.intel.com.

11.0 Reference Schematics

The following pages contain reference schematics for the 82541ER GbE controller.


REVISIONS
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DESCRIPTION
DATE
82541ER
Reference Design
15mm x 15mm BGA
1mm pitch
Page 2: Block Diagram
Page 3: Symbol
Page 4: PHY Interface
Page 5: Alternate Copper AFE
Page 6: Power Regulation, LEDs, and Crystal
Page 7: External Voltage Regulator
Page 8: LAN Disable
PBA NO.
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DATE
DRAWN
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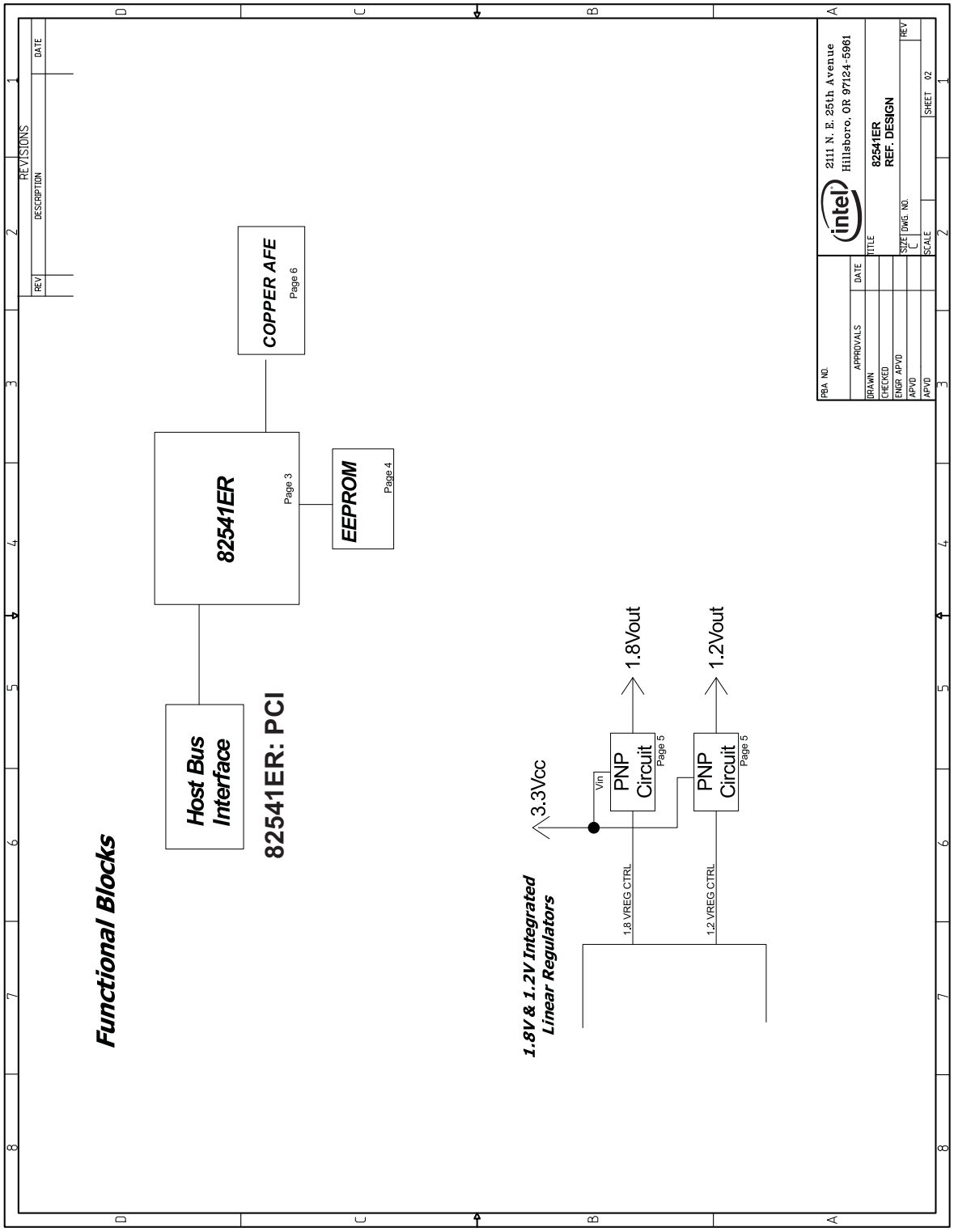
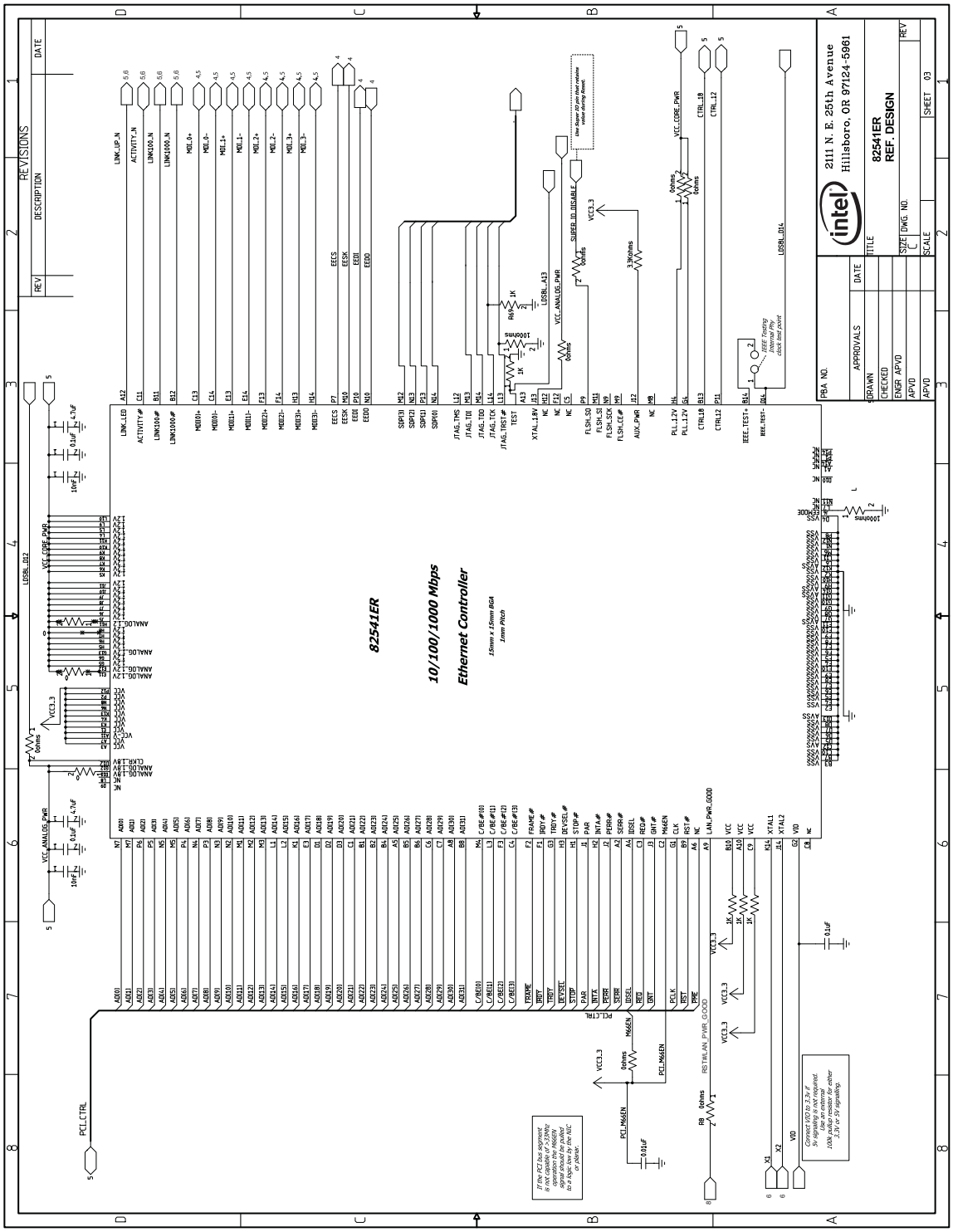
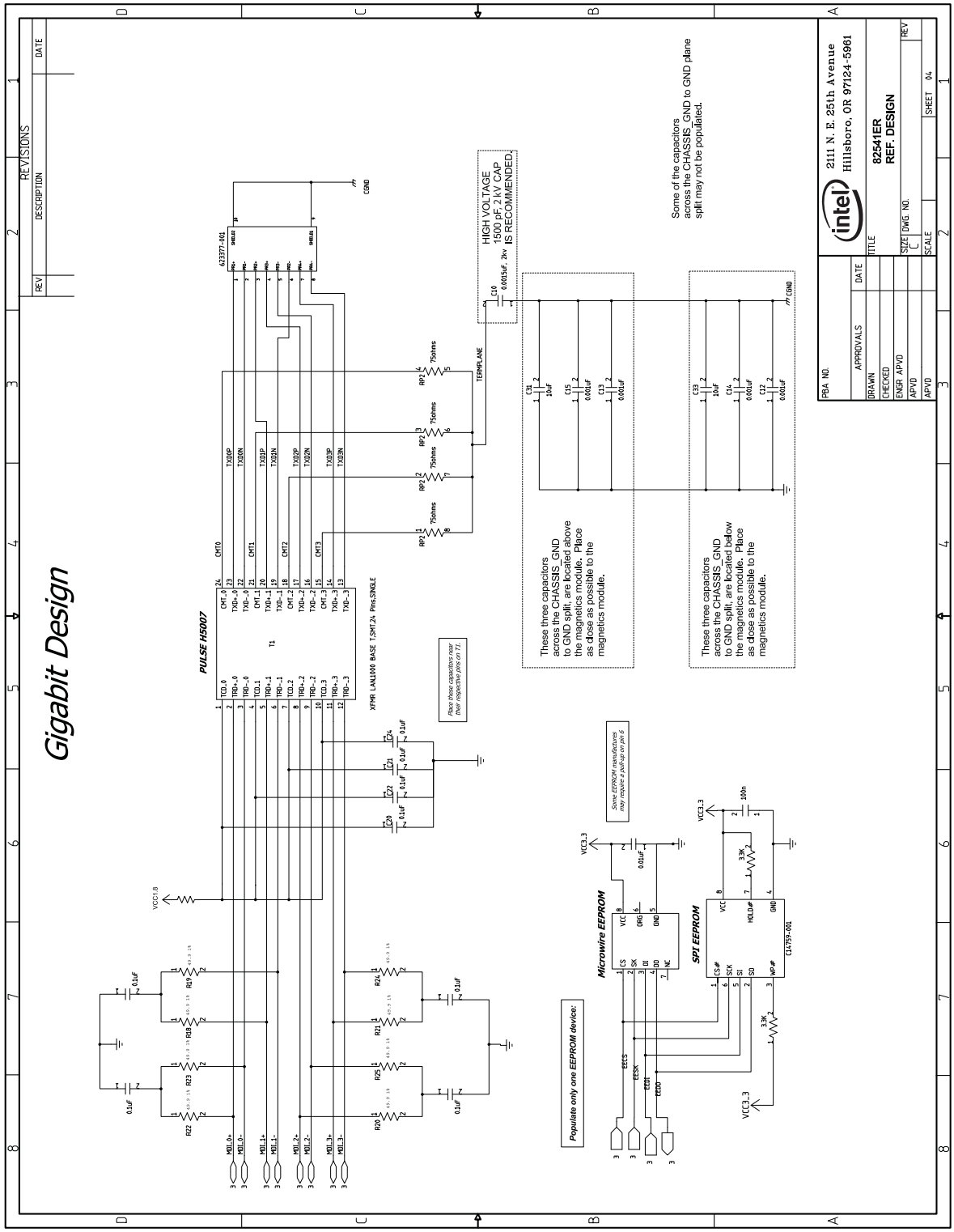
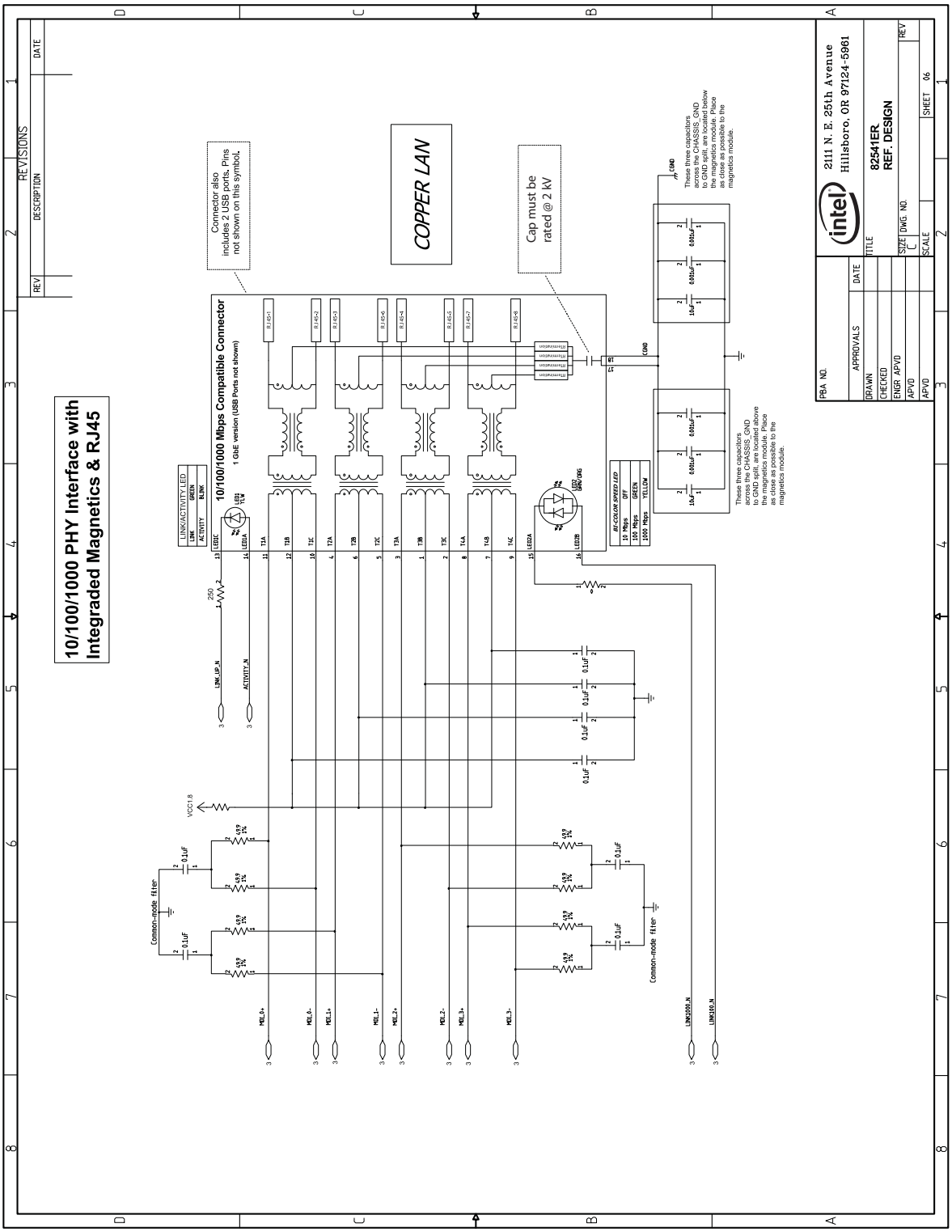
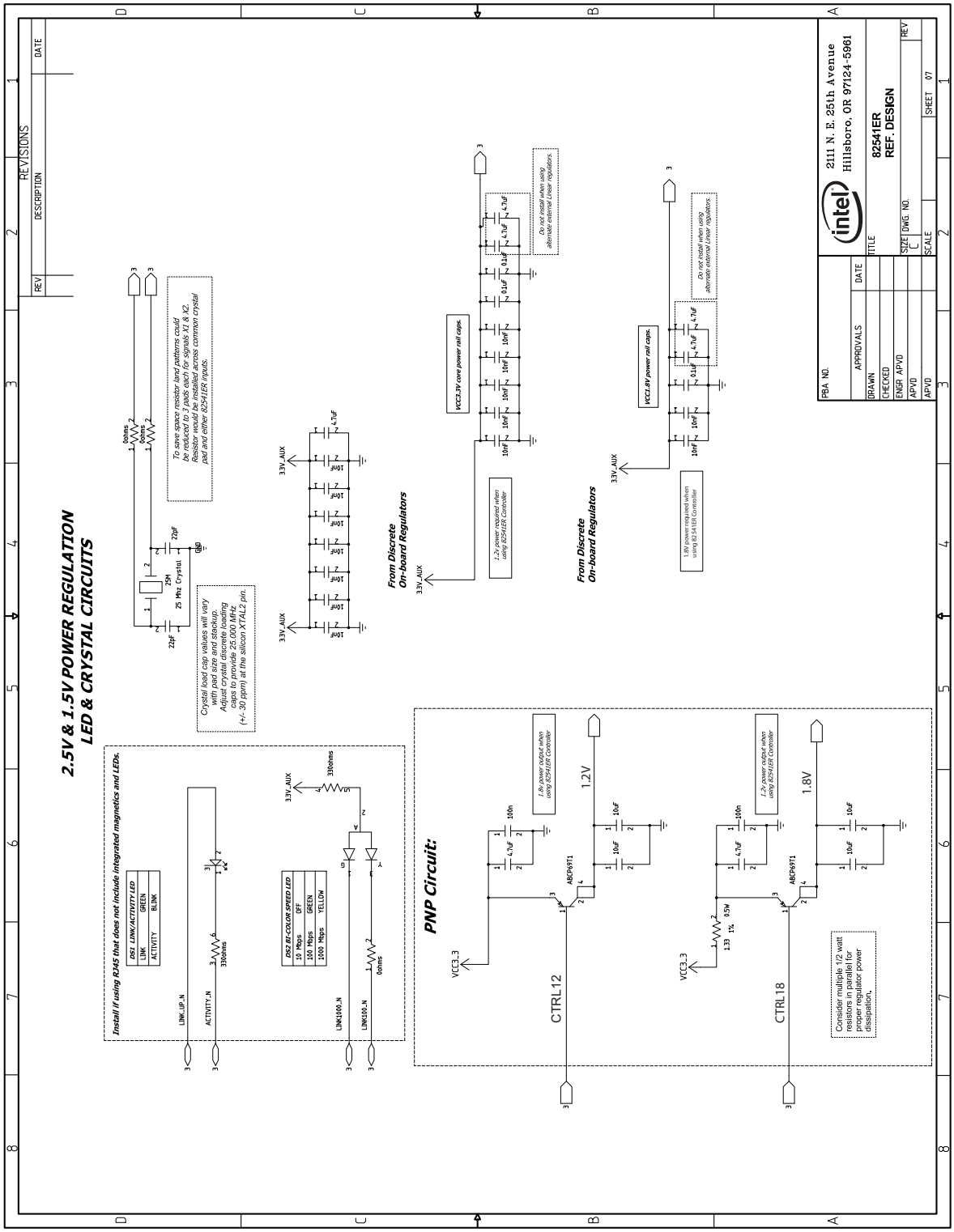
ENGR APVD
APVD
APVD
2111 N. E. 25th Avenue
Hillsboro, OR 97124-5961
TITLE
82541ER
REF. DESIGN
SIZE
C
DWG. NO.
REV
SCALE
SHEET 01


REVISIONS
REV
DESCRIPTION
DATE
Functional Blocks
Host Bus Interface
82541ER: PCI
82541ER
Page 3
EEPROM
Page 4
COPPER AFE
Page 6
1.8V & 1.2V Integrated Linear Regulators
3.3Vcc
Vin
PNP Circuit
Page 5
1.8Vout
1.8 VREG CTRL
PNP Circuit
Page 5
1.2Vout
1.2 VREG CTRL
PBA NO.
APPROVALS
DATE
DRAWN
CHECKED
ENGR APVD
APVD
APVD
TITLE
82541ER
REF. DESIGN
SIZE
C
DWG. NO.
REV
SCALE
SHEET 02
2111 N. E. 25th Avenue
Hillsboro, OR 97124-5961


82541ER
10/100/1000 Mbps
Ethernet Controller
15mm x 15mm BGA
1mm Pitch
2111 N. E. 25th Avenue
Hillsboro, OR 97124-5961
82541ER
REF. DESIGN
REVISIONS
PCI_CTRL
RST#LAN_PWR_GOOD
LAN_PWR_GOOD
VCC_CORE_PWR
VCC_ANALOG_PWR
VCC3.3
LDSBL_D12
LDSBL_D14
LDSBL_A13
SUPER_ID_DISABLE
IEEE_TEST+
IEEE_TEST-
PCI_M66EN
SHEET 03


Gigabit Design
REVISIONS
REV
DESCRIPTION
DATE
PULSE H5007
XFMR LAN1000 BASE T,SMT,24 Pins,SINGLE
HIGH VOLTAGE
1500 pF, 2 kV CAP
IS RECOMMENDED.
Some of the capacitors
across the CHASSIS_GND to GND plane
split may not be populated.
These three capacitors
across the CHASSIS_GND
to GND split, are located above
the magnetics module. Place
as close as possible to the
magnetics module.
These three capacitors
across the CHASSIS_GND
to GND split, are located below
the magnetics module. Place
as close as possible to the
magnetics module.
Place these capacitors near
their respective pins on T1.
Some EEPROM manufactures
may require a pull-up on pin 6
Microwire EEPROM
SPI EEPROM
Populate only one EEPROM device:
2111 N. E. 25th Avenue
Hillsboro, OR 97124-5961
82541ER
REF. DESIGN
SHEET 04


10/100/1000 PHY Interface with Integraded Magnetics & RJ45
COPPER LAN
Connector also includes 2 USB ports. Pins not shown on this symbol.
Cap must be rated @ 2 kV
10/100/1000 Mbps Compatible Connector
1 GbE version (USB Ports not shown)
LINK/ACTIVITY LED
LINK GREEN
ACTIVITY BLINK
10 Mbps OFF
100 Mbps GREEN
1000 Mbps YELLOW
These three capacitors across the CHASSIS_GND to GND split, are located below the magnetics module. Place as close as possible to the magnetics module.
Common-mode filter
MDI0+
MDI0-
MDI1+
MDI1-
MDI2+
MDI2-
MDI3+
MDI3-
LINK1000_N
LINK100_N
LINK_UP_N
ACTIVITY_N
VCC1.8
PBA NO.
APPROVALS
DRAWN
CHECKED
ENGR APVD
APVD
APVD
DATE
TITLE
82541ER
REF. DESIGN
SIZE C
DWG. NO.
REV
SCALE
SHEET 06
2111 N. E. 25th Avenue
Hillsboro, OR 97124-5961
REVISIONS
REV
DESCRIPTION
DATE


2.5V & 1.5V POWER REGULATION
LED & CRYSTAL CIRCUITS
REVISIONS
REV
DESCRIPTION
DATE
Install if using RJ45 that does not include integrated magnetics and LEDs.
DS1 LINK/ACTIVITY LED
LINK GREEN
ACTIVITY BLINK
DS2 BI-COLOR SPEED LED
10 Mbps OFF
100 Mbps GREEN
1000 Mbps YELLOW
LINK_UP_N
ACTIVITY_N
LINK1000_N
LINK100_N
330ohms
0ohms
To save space resistor land patterns could be reduced to 3 pads each for signals X1 & X2. Resistor would be installed across common crystal pad and either 82541ER inputs.
Crystal load cap values will vary with pad size and stackup. Adjust crystal discrete loading caps to provide 25.000 MHz (+/- 30 ppm) at the silicon XTAL2 pin.
25 Mhz Crystal
22pF
GND
33V_AUX
From Discrete On-board Regulators
VCC3.3V core power rail caps.
1.2v power required when using 82541ER Controller
Do not install when using alternate external Linear regulators.
VCC1.8V power rail caps.
1.8V power required when using 82541ER Controller
PNP Circuit:
VCC3_3
CTRL12
CTRL18
1.2V
1.8V
ABCP69T1
1.8v power output when using 82541ER Controller
1.2v power output when using 82541ER Controller
Consider multiple 1/2 watt resistors in parallel for proper regulator power dissipation.
PBA NO.
APPROVALS
DATE
DRAWN
CHECKED
ENGR APVD
APVD
APVD
2111 N. E. 25th Avenue
Hillsboro, OR 97124-5961
TITLE
82541ER
REF. DESIGN
SIZE
C
DWG. NO.
REV
SCALE
SHEET 07

Appendix A Measuring LAN Reference Frequency Using a Frequency Counter

A.1 Background

To comply with IEEE specifications for 10/100/1000Base-T Ethernet LAN, the transmitter reference frequency must be correct and accurate within ±50 parts per million (ppm).

Note: Intel recommends a frequency tolerance of ±30 (ppm).

Most Intel LAN devices will operate properly with a 25.000 MHz reference crystal, provided it meets the recommended requirements for frequency stability, equivalent series resistance at resonance (ESR), and load capacitance.

Most circuits for series resonant crystals include two discrete capacitors (typically C1 and C2), with values between 5 pF and 36 pF.

The most accurate way to determine the appropriate value for the discrete capacitors is to install the approximately correct values for C1 and C2. Next, a frequency counter should be used to measure the transmitter reference frequency (or transmitter reference clock).

- If the transmitter reference frequency is more than 20 ppm below the target frequency, then the values for C1 and C2 are too big and should be decreased.
- If the transmitter reference frequency is more than 20 ppm above the target frequency, then the values for C1 and C2 are too small and should be increased.

This Appendix provides instructions and illustrations that explain how to use a frequency counter and probe to determine the Ethernet LAN device transmit center frequency. An example describing how to calculate the frequency accuracy of the measured and averaged center frequency with respect to the target center frequency is also included.

A.2 Required Test Equipment

- Tektronix CMC-251, or similar high resolution, digital counter
- Tektronix P6246, or similar high bandwidth, low capacitance (less than 1 pF) probe
- Tektronix 1103, or similar probe power supply or probe amplifier
- BNC, 50 Ω coaxial cable (less than 6 feet long)
- System with power supply and test software for the LAN circuit to be tested

A.3 Indirect Probing Method

Almost all Intel LAN silicon that support 1000BASE-T Ethernet can provide a buffered 125 MHz clock, which can be used for indirect probing of the transmitter reference clock. The buffered 125 MHz clock will be a 5X multiple of the crystal circuit's reference frequency (Figure 7).

Different LAN devices may require different register settings, to enable the buffered 125 MHz reference frequency. Please obtain the settings or instructions that are appropriate for the GbE controller you are using.

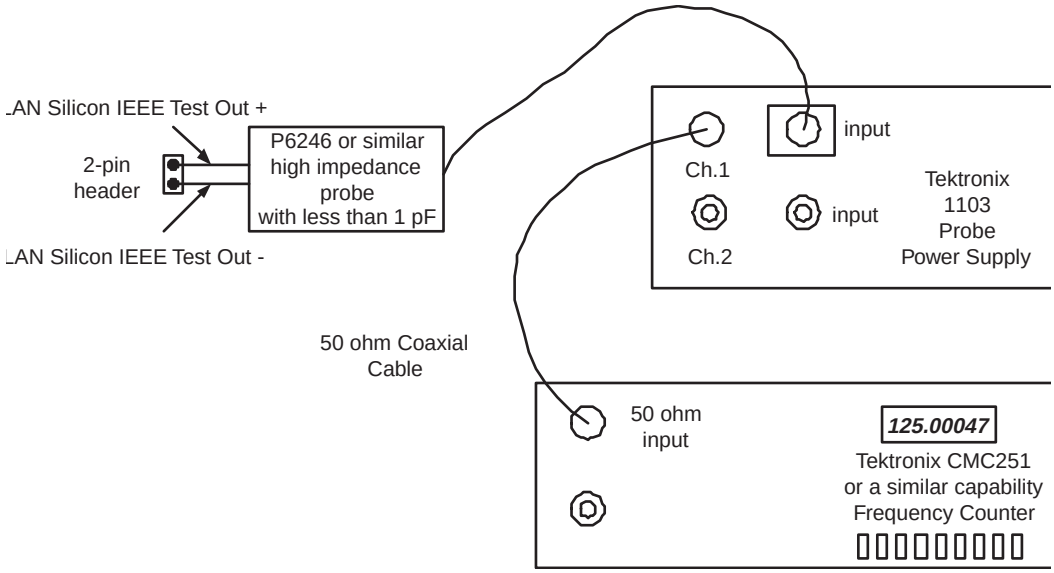


Figure 7. Indirect Probing Setup

A.4 Indirect Frequency Measurement and Frequency Accuracy Calculation Steps

1. Make sure the system BIOS has the GbE controller enabled.
2. Connect the test equipment as shown in Figure 7.
3. Using the appropriate controls for your model of high resolution digital counter, make sure it can display ~125.0000 MHz with at least four decimal places frequency resolution.
4. Enable the 125 MHz buffered reference clock.
5. Determine the center reference frequency as accurately as possible. This can be done by taking 30 to 50 different readings using the frequency counter and then calculating the average results of the readings.
6. Calculate the accuracy of the measured and averaged center frequency with respect to an ideal 125.0000 MHz reference frequency.

$$\text{FrequencyAccuracy(ppm)} = \frac{(x - y)}{(y / 1000000)}$$

where x = Average measured frequency in Hertz and
y = Ideal reference frequency in Hertz

Example 1.

Given: The measured averaged center frequency is 124.99942 MHz (or 124,999,420 Hertz).

$$\text{FrequencyAccuracy(ppm)} = \frac{(124999420 - 125000000)}{(125000000/1000000)} = -4.64\text{ppm}$$

Example 2.

Given: The measured averaged center frequency is 125.00087 MHz (or 125,000,870 Hertz).

$$\text{FrequencyAccuracy(ppm)} = \frac{(125000870 - 125000000)}{(125000000/1000000)} = 6.96\text{ppm}$$

Note: The following items should be noted for an ideal reference crystal on a typical printed circuit board.

- If the transmitter reference frequency is more than 8 ppm below the target frequency, then the values for C1 and C2 are too big and they should be decreased. When tests are performed across temperature, it may be acceptable for the center frequency deviation to be a little greater than 8 ppm.
- If the transmitter reference frequency is more than 8 ppm above the target frequency, then the values for C1 and C2 are too small and they should be increased. When tests are performed across temperature, it may be acceptable for the center frequency deviation to be a little greater than 8 ppm.

Appendix B GigConf.exe Register Settings for 82541ER Devices

The following steps describe the indirect probing test method using GigConf.exe for 82541ER devices.

1. Boot to DOS using a DOS Boot Diskette.
2. Launch Gigconf from the diskette (gigconf.exe).
3. Select the Intel network connection to be measured.
   a. If multiple adapters are installed, use the arrow keys to navigate to highlight the selected adapter and press Enter.
4. Select Registers by pressing “R”.
5. Select PHY Registers by pressing “P”.
6. Use the arrow keys to navigate to the value listed next to address 0000.
7. Press Enter when the value is highlighted and then use Backspace to clear out the current value.
8. Type “0100” for the value and then press Enter.
9. Navigate to the value listed next to address 0012.
10. Press Enter to select the highlighted value and use Backspace to clear the current value.
11. Type “8000” for the value and then press Enter.
12. Navigate to the Set Address field on the right side of the screen (use the right arrow key)
13. Press Enter to select the highlighted value and then use Backspace to clear out the current value.
14. Type “4011” for the value and then press Enter.
15. This changes the PHY register screen and updates it with new addresses and values.
16. Use the arrow keys to navigate to the value for address 4011.
17. Press Enter when the value is highlighted and then use Backspace to clear the current value.
18. Type “8000” for the value and then press Enter.
19. Use the right arrow key to navigate to the Set Address field on the right side of the screen.
20. Press Enter when the value is highlighted and use Backspace to clear the current value.
21. Enter “2F5B” (capital letters are not required) for the address and then press Enter.
22. Use the arrow keys to navigate to the value for address “2F5B”.
23. Press Enter when the value is highlighted and then use Backspace to clear the current value.
24. Type “0003” for the value and then press Enter.
25. Use the right arrow key to navigate to the Set Address field on the right side of the screen.
26. Press Enter when the value is highlighted and then use Backspace to clear the current value.

Note: This page intentionally left blank.